MFS1S50-H0xxV 200Gb/s QSFP56 to 2x100Gb/s QSFP56 Low Latency MMF AOC Product Specifications

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Introduction

NVIDIA® MFS1S50 is a QSFP56 VCSEL-based (Vertical Cavity Surface-Emitting Laser), cost-effective 200Gb/s to 2 x 100Gb/s active optical splitter cable (AOC) designed for use in 200Gb/s InfiniBand (IB) HDR (High Data Rate) and 200GbE systems.

The MFS1S50 cable is compliant with SFF-8665 for the QSFP56 pluggable solution. It provides connectivity between system units with a 200Gb/s connector on one side and two separate 100Gb/s connectors on the other side, such as a switch and two servers. The cable connects data signals from each of the 4 MMF (Multi Mode Fiber) pairs on the single QSFP56 end to the dual pair of each of the QSFP56 multiport ends. Each QSFP56 end of the cable comprises an EEPROM providing product and status monitoring information, which can be read by the host system.

NVIDIA's unique-quality cable solutions provide power-efficient connectivity for data center interconnects. It enables higher port bandwidth, density and configurability at a low cost, and reduced power requirement in the data centers.

Rigorous production testing ensures the best out-of-the-box installation experience, performance and durability.

Note

Images are for illustration purposes only. Product labels, colors, and lengths may vary.

Key Features

- Supports IBTA IB HDR and 200GbE
- 200Gb/s HDR to 2x100Gb/s HDR100 data rate
- 200GbE to 2x100GbE data rate
- 4x 50Gb/s PAM4 modulation
- Programmable Rx output amplitude and pre-emphasis
- SFF-8665 compliant QSFP56 port
- Single 3.3V power supply
- 4.5W power consumption (typ., 200G end)
- Up to 30m length
- Hot pluggable
- RoHS compliant
- SFF-8636 compliant I^2C management interface

Pin Description

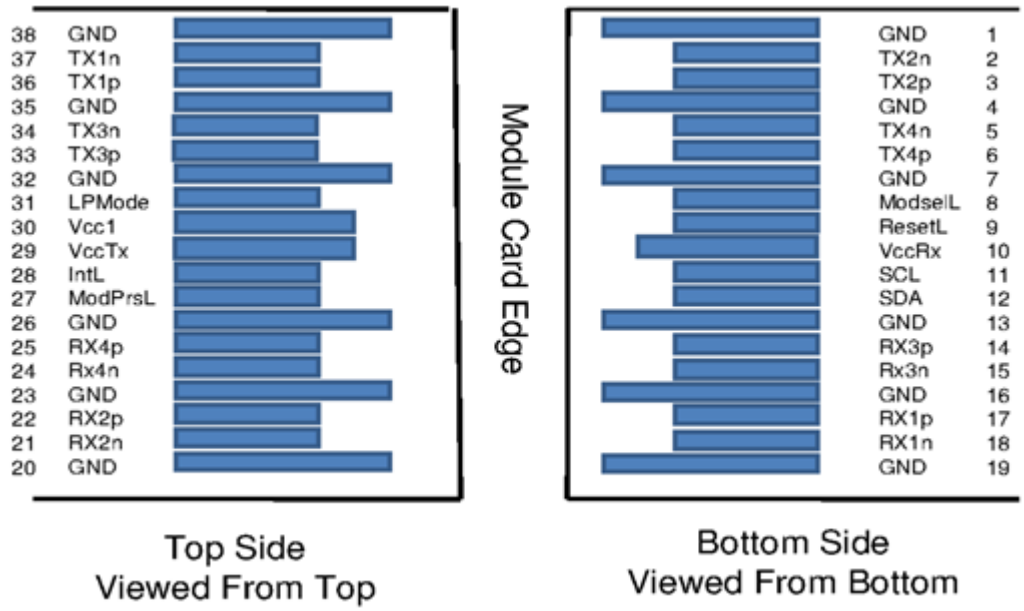
The Active Optical Cable (AOC) pin assignment is SFF-8679 compliant.

QSFP56 Pin Description 200Gb/s End

Pin	Symbol	Description	Pin	Symbol	Description
1	Ground	Ground	20	Ground	Ground
2	Tx2n	Connected to Port 1 lane Rx2 Inverted Data	21	Rx2n	Connected to Port 1 lane Tx2 Inverted Data
3	Tx2p	Connected to Port 1 lane Rx2 Non-Inverted Data	22	Rx2p	Connected to Port 1 lane Tx2 Non-Inverted Data
4	Ground	Ground	23	Ground	Grounds
5	Tx4n	Connected to Port 2 lane Rx2 Non-Inverted Data	24	Rx4n	Connected to Port 2 lane Tx2 Inverted Data
6	Tx4p	Connected to Port 2 lane Rx2 Inverted Data	25	Rx4p	Connected to Port 2 lane Tx2 Non-Inverted Data
7	Ground	Ground	26	Ground	Ground
8	Mod-SelL	Cable Select	27	ModPrsL	Cable Present
9	ResetL	Cable Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3V Power supply receiver	29	Vcc Tx	+3.3V Power supply transmitter
11	SCL	2-wire serial interface clock	30	Vcc1	+3.3V Power Supply
12	SDA	2-wire serial interface data	31	LPMode	Low Power Mode

Pin	Symbol	Description	Pin	Symbol	Description
13	Ground	Ground	32	Ground	Ground
14	Rx3p	Connected to Port 2 lane Tx1 Non-Inverted Data	33	Tx3p	Connected to Port 2 lane Rx1 Non-Inverted Data
15	Rx3n	Connected to Port 2 lane Tx1 Inverted Data	34	Tx3n	Connected to Port 2 lane Rx1 Inverted Data
16	Ground	Ground	35	Ground	Ground
17	Rx1p	Connected to Port 1 lane Tx1 Non-Inverted Data	36	Tx1p	Connected to Port 1 lane Rx1 Non-Inverted Data
18	Rx1n	Connected to Port 1 lane Tx1 Inverted Data	37	Tx1n	Connected to Port 1 lane Rx1 Inverted Data
19	Ground	Ground	38	Ground	Ground

QSFP56 Module Pad Layout



QSFP56 Pin Description 100Gb/s End

Pin	Symbol	Description	Pin	Symbol	Description
1	Ground	Ground	20	Ground	Ground
2	Tx2n	Connected to lane Rx2 Inverted Data	21	Rx2n	Connected to lane Tx2 Inverted Data
3	Tx2p	Connected to lane Rx2 Non-Inverted Data	22	Rx2p	Connected to lane Tx2 Non-Inverted Data
4	Ground	Ground	23	Ground	Grounds
5	Not connected	Not connected	24	Not connected	Not connected
6	Not connected	Not connected	25	Not connected	Not connected
7	Ground	Ground	26	Ground	Ground
8	Mod-SelL	Cable Select	27	ModPrsL	Cable Present
9	ResetL	Cable Reset	28	IntL	Interrupt
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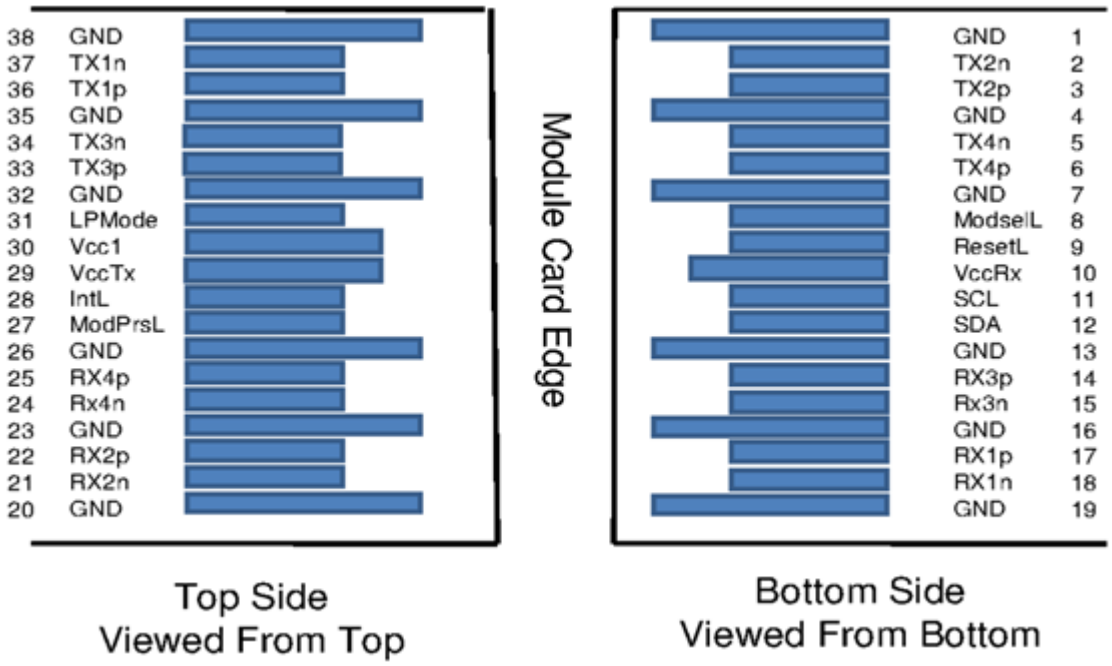
18	Rx1n	Connected to lane Tx1 Inverted Data	37	Tx1n	Connected to lane Rx1 Inverted Data
19	Ground	Ground	38	Ground	Ground

QSFP56 Module Pad Layout

The pinout of the 100Gb/s ends of the cable is identical to the 200Gb/s end except that RF lanes 3 and 4 (pins 5, 6, 14, 15, 24, 25, 33, 34) are not used.



Control Signals

This transceiver is SFF-8636 compliant. This means that the control signals shown in the pad layout support the following functions:

Name	Function	Description
ModPrsL	Output, asserted low	Module Present pin, grounded inside the module. Terminated with pull-up in the host system. Asserted low when the transceiver is inserted, whereby the host detects the presence of the transceiver.
ModSelL	Input, asse	Module Select input pin, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.

Name	Function	Description
	rted Low	
ResetL	Input, asserted Low	Reset input pin, pulled high in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. During reset the host shall disregard all status bits until the module indicates completion of the reset interrupt by asserting IntL signal low with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module completes the reset interrupt without requiring a reset.
LPMode	Input, asserted high	Low Power Mode input, pulled up inside the module. The transceiver starts up in low-power mode, i.e. <1.5 W with the two-wire interface active. The host system can read the power class declaration from the transceiver and determine if it has enough power to enable the high-speed operation/high power mode of the transceiver. This can be done by asserting LPMode low or by use of the Power_over-ride and Power_set control bits (Address A0h, byte 93 bits 0,1).
IntL	Output, asserted low	Interrupt Low is an open-collector output, terminated high in the host system. A “Low” indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface. The INTL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’.

The low-speed signals are Low Voltage TTL (LVTTL) compliant (except for SCL and SDA signals).

Diagnostics and Other Features

The transceiver complies with the SFF-8665 specification and has the following key features:

Physical layer link optimization:

- Programmable Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-emphasis

- Tx/Rx CDR control

  by default enabled for 100 GbE operation, disable it for 40G operation

Digital Diagnostic Monitoring (DDM):

- Rx receive optical power monitor for each lane
- Tx transmit optical power monitor for each lane
- Tx bias current monitor for each lane
- Supply voltage monitor
- Transceiver case temperature monitor
- Warning and Alarm thresholds for each DDM function (not user changeable)

Other SFF-8636 functions and interrupt indications:

- Tx & Rx LOS indication
- Tx & Rx LOL indication
- Tx fault indication

LOS, LOL, and Tx Fault status flags can be read via the two-wire management interface and are jointly transmitted via the IntL output pin. Relevant advertisement, threshold, and readout registers are found in the SFF-8636 MSA.

Specifications

Absolute Maximum Specifications

Absolute maximum ratings are those beyond which damage to the device may occur.

Prolonged operation between the operational specifications and absolute maximum ratings is not intended and may cause permanent device degradation.

Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply voltage	-0.3	3.6	V
Data input voltage	-0.3	3.465	V
Control input voltage	-0.3	4.0	V
Damage Threshold	3.4	---	dBm

Environmental Specifications

This table shows the environmental specifications for the product.

Parameter	Min	Max	Units
Storage temperature	-40	85	°C

Operational Specifications

This section shows the range of values for normal operation. The host board power supply filtering should be designed as recommended in the SFF Committee Spec.

Parameter	Min	Typ	Max	Units	Notes
Supply voltage (V_{CC})	3.135	3.3	3.465	V	---

Parameter	Min	Typ	Max	Units	Notes
Power consumption 200Gb/s end	---	4.5	5.0	W	---
Power consumption 100Gb/s end	---	3.0	3.5	W	---
Supply noise tolerance (10Hz – 10MHz)	66	---	---	mVpp	---
Operating case temperature	0	---	70	°C	---
Operating relative humidity	5	---	85	%	---

Electrical Specifications

Parameter (per lane)	Min	Typ	Max	Units
Signaling rate	-100 ppm	53.125	+100 ppm	GBd
Differential data input swing at TP1a	TBD	---	900	mVpp
Differential data output swing at TP4	---	---	900	mVpp
Near-end ESMW	0.265	---	---	UI
Near-end output eye height	70	---	---	mVpp
Output transition time, 20% to 80%	9.5	---	---	ps

Notes:

- Multiple clock domains are supported only on line-side Rx. Host side Rx supports a single clock domain only.
- QSFP Tx CDR lock can only occur if Tx lane 4 is transmitting data.

Electrostatic Discharge (ESD)

This product is compatible with ESD levels in typical data center operating environments and certified in accordance with the standards listed in the Regulatory Compliance Section. The product is shipped with protective caps on all connectors to protect it during shipping. In normal handling and operation of high-speed cables and optical transceivers, ESD is of concern during insertion into the QSFP cage of the server/switch. Hence, standard ESD handling precautions must be observed. These include use of grounded wrist/shoe straps and ESD floor wherever a cable/transceiver is extracted/inserted. Electrostatic discharges to the exterior of the host equipment chassis after installation are subject to system level ESD requirements.

Handling and Cleaning

The transceiver can be damaged by exposure to current surges and over voltage events. Take care to restrict exposure to the conditions defined in Absolute Maximum Ratings. Observe normal handling precautions for electrostatic discharge-sensitive devices. The transceiver is shipped with dust caps on both the electrical and the optical port. The cap on the optical port should always be in place when there is no fiber cable connected. The optical connector has a recessed connector surface which is exposed whenever it has no cable nor cap.

Prior to insertion of the fiber cable, clean the cable connector to prevent contamination from it. The dust cap ensures that the optics remain clean and no additional cleaning should be needed. In the event of contamination, standard cleaning tools and methods should be used. Liquids must not be applied.

Interoperability

For configurations tested with the AOCs please refer to the system level product (SLP) qualification report.

Rate Select

The AOC supports rate select, which is controlled by writing to registers 0x57-0x58. Two bits are assigned for each receiver lane in byte 0x57 (87dec, Rxn_Rate_Select) and two bits for each transmitter lane in byte 0x58 (88dec, Txn_Rate_Select) to specify up to four bitrates, as defined in SFF-8636 Rev 2.9.2 Table 6-5 XN_RATE_SELECT ENCODINGS. All four lanes are required to have the same rate select value.

The below table specifies the rate for each rate select setting.

Rate Select Encodings

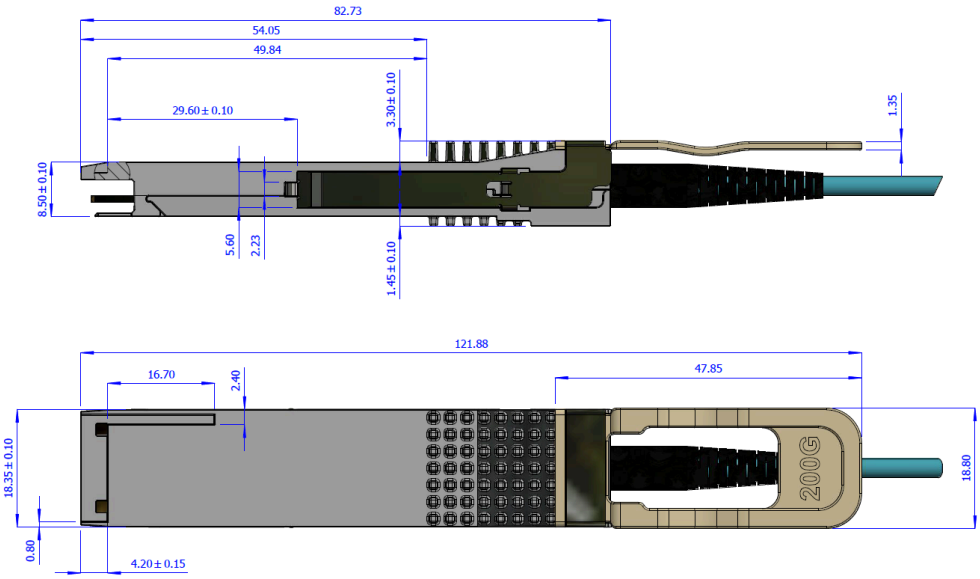
Rate Select Value	Operating Rate (GBd)
01	10.31250 NRZ
10	25.78125 NRZ
11	26.56250 PAM4

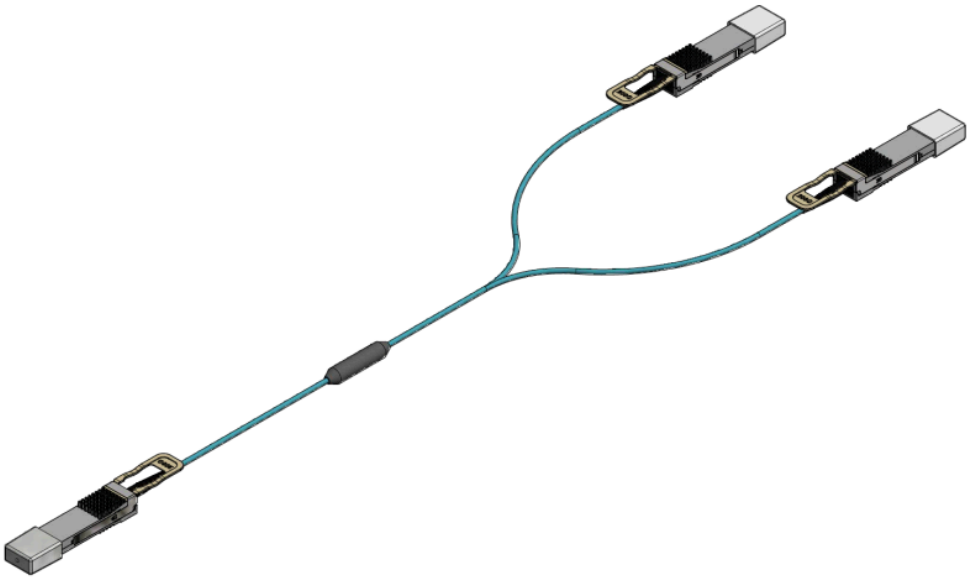
Mechanical Specifications

Parameter	Value		Units
Diameter	3 +/-0.2		mm
Minimum bend radius	30		mm
Length tolerance	length < 5 m	+300 /-0	mm
	5 m ⩽ length < 50 m	+500 / -0	
	50 m ⩽ length	+1000 /-0	
Cable color	Aqua		---

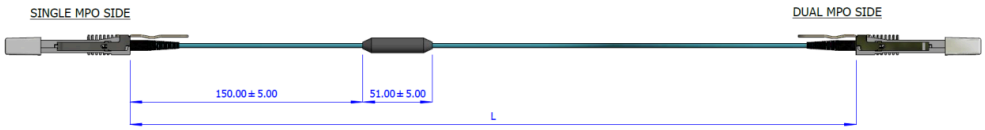
Mechanical Dimensions

Option 1

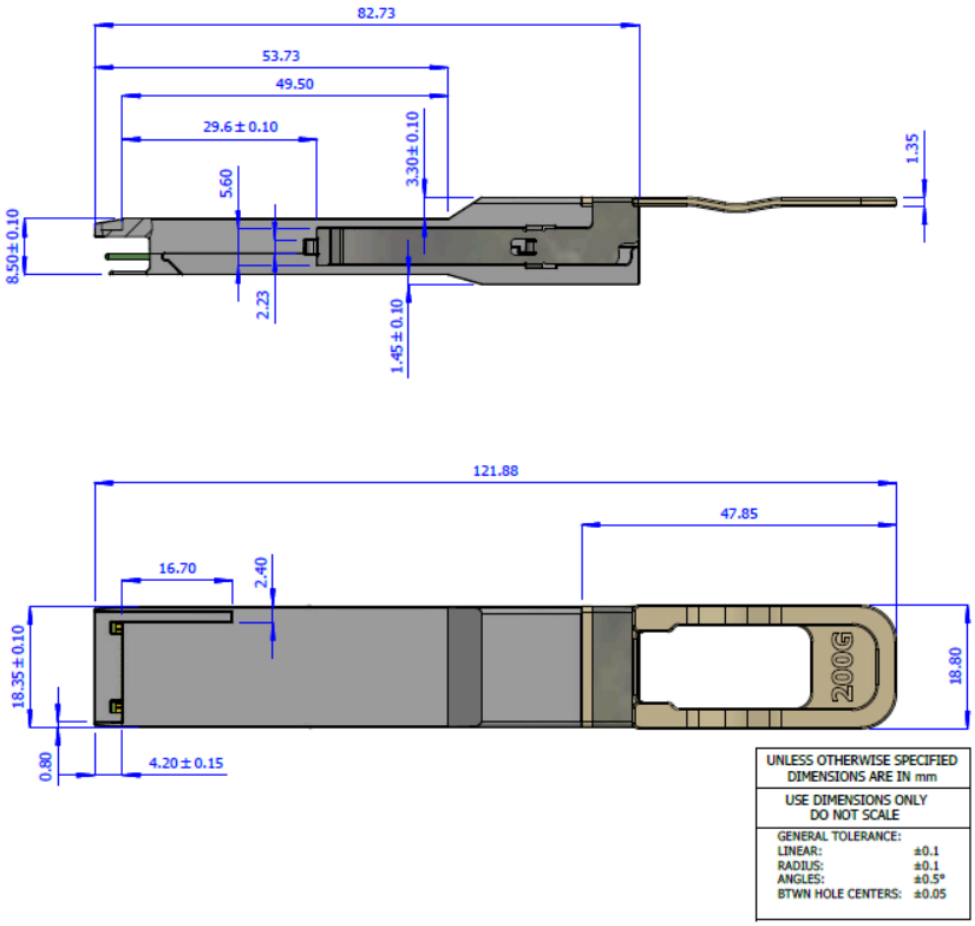




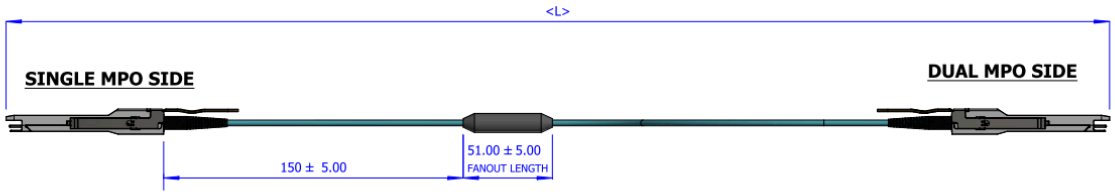
Splicing Point and Cable Length



Option 2



Splicing Point and Cable Length



Note

Option 1+2 refers to parts with slightly different designs and may have different pull tab shape, color, and transceiver top.

Connectivity Schematic

200Gb/s Side	2x100Gb/s Side
	Port 1
TX1	RX1
RX1	TX1
TX2	RX2
RX2	TX2
	Port 2
TX3	RX1
RX3	TX1
TX4	RX2
RX4	TX2

Labels

The following labels are applied on the AOC backshells:

200Gb/s Backshell Label

(sample illustration)

100Gb/s Backshell Label

(sample illustration)

> **Note**
>
> Images are for illustration purposes only. Product labels, colors, and lengths may vary.

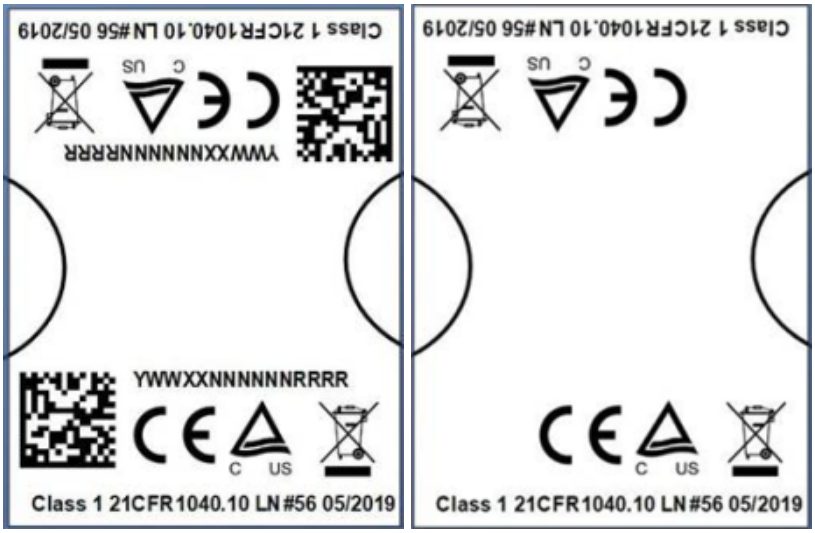
Backshell Label Legend

Symbol	Meaning	Notes
PN – Part Number		
xx	Length	Meter
SN – Serial Number		
MT	Manufacturer name	2 characters, e.g. MT
YY	Year of manufacturing	2 digits
WW	Week of manufacturing	2 digits
XX	Manufacturer site	2 characters

Symbol	Meaning	Notes
SSSSS	Serial number	5 digits for serial number, starting from 00001. Reset at start of week to 00001.
Miscellaneous		
ZZ	HW and SW revision	2 alpha-numeric characters
YYYY	Year of manufacturing	4 digits
MM	Month of manufacturing	2 digits
DD	Day of manufacturing	2 digits
COO	Country of origin	E.g. China or Malaysia
XXm	Cable length	Meter
	Quick response code	Serial number (MTYYWWXXSSSSS)

The following label is applied on the cable's jacket:

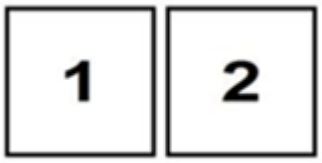
Fiber Cable Jacket Label



(sample illustration)

Note:The serial number and barcode are for internal use only. Different layouts of this label apply to different production series. It has no effect on the cable's performance nor function.

Splitter Cable Labels Identifying the 2 QSFP56 Tails



(sample illustration)

Regulatory Compliance and Classification

The laser module is classified as class I according to IEC 60825-1, IEC 60825-2 and 21 CFR 1040 (CDRH).

- Safety: CB, cTUVus, CE
- EMC: CE, FCC, ICES, RCM, VCCI

Ask your NVIDIA FAE for a zip file of the certifications for this product.

FCC Class A Notice

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Ordering Information

Ordering Part Number	Description
MFS1S50-H003V	NVIDIA active optical splitter cable, 200Gbps to 2x100Gbps, QSFP56 to 2x QSFP56, 3m
MFS1S50-H005V	NVIDIA active optical splitter cable, 200Gbps to 2x100Gbps, QSFP56 to 2x QSFP56, 5m
MFS1S50-H010V	NVIDIA active optical splitter cable, 200Gbps to 2x100Gbps, QSFP56 to 2x QSFP56, 10m
MFS1S50-H015V	NVIDIA active optical splitter cable, 200Gbps to 2x100Gbps, QSFP56 to 2x QSFP56, 15m
MFS1S50-H020V	NVIDIA active optical splitter cable, 200Gbps to 2x100Gbps, QSFP56 to 2x QSFP56, 20m
MFS1S50-H030V	NVIDIA active optical splitter cable, 200Gbps to 2x100Gbps, QSFP56 to 2x QSFP56, 30m

Refer here for the cable length definition.

References

1. LinkX_Memory_Map_Application_Note (MLNX-15-5926)
2. NVIDIA_Cable_Management_Guidelines_and_FAQs_Application_Note (MLNX-15-3603)

For documentation, please contact your sales representative or the Support team.

Document Revision History

Revision	Date	Description
1.4	Nov. 2024	Updated splitting point mechanical drawing.
1.3	Oct. 2023	• Added 200GbE mentions • Updated descriptions in ordering information table
1.2	Aug. 2022	Reformatted and rebranded; migrated to HTML file.
1.1	May 2012	Updated Mechanical Drawings.
1.0	Nov., 2021	Initial revision

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