100G QSFP28 ZR4 80km LAN-WDM Transceiver

CC-QKKLL8L-SD

Features

- Supports 103Gbps
- Up to 80km for G.652 SMF
- Single 3.3V Power Supply and Power dissipation < 7.5W
- 4x28Gbps EML-based LAN-WDM cooling transmitter
- SOA+PIN and TIA array on the receiver side
- 4x28Gbps retimed electrical interface
- Duplex LC receptacles
- I^2C interface with integrated Digital Diagnostic Monitoring
- Operating Case Temperature: -40°C ~85°C

Applications

- 100GBASE-ZR4 Ethernet

Standard

- Compliant with QSFP28 MSA Specification
- Class 1 FDA and IEC60825-1 Laser Safety Compliant

Product Description

CC-QKKLL8L-SD is designed for 103 Gigabit Ethernet links over 80km single mode fiber. It is compliant with IEEE 802.3ba. Digital diagnostics functions are available via an I2C interface, as specified by the QSFP28 MSA.

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Order Information

Part No.	Data Rate	Fiber	Distance	Interface	Temp.	DDMI
CC-QKKLL8L-SD	103Gbps	SMF	80km	LC	-40℃~85℃	YES

Optical and Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Transmitter					
Signaling Rate, each lane	BRAVE		25.78		Gbps
Data Rate Variation		-100		+100	Ppm
Lane_0 Center Wavelength	λC0	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λC1	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λC2	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λC3	1308.09	1309.14	1310.19	nm
Side-mode Suppression ratio	SMSR	30			dB
Total Average Output Power	Po			12.5	dBm
Average Launch Power each lane*(Note1)	Peach	2		6	dBm
Optical Modulation Amplitude (OMA) each lane	TXOMA			3.6	dBm
Average launch power of OFF transmitter each lane	Poff			-30	dBm
Transmitter and Dispersion Penalty (TDP), each lane	TDP			2.5	dB
Extinction Ratio, each lane	ER	8			dB
Relative Intensity Noise	RIN			-130	dB/hz
Transmitter Reflectance	REFLT			-12	dB
Optical Return Loss Tolerance				20	dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}*(Note2)		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
Receiver					
Signaling rate, each lane	BRAVE		25.78		Gbps
Data Rate Variation		-100		+100	Ppm
Lane_0 Center Wavelength	λC0	1294.53	1295.56	1296.59	nm
Lane_1 Center Wavelength	λC1	1299.02	1300.05	1301.09	nm
Lane_2 Center Wavelength	λC2	1303.54	1304.58	1305.63	nm
Lane_3 Center Wavelength	λC3	1308.09	1309.14	1310.19	nm

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Average Receive Power, each lane *(Note3)	RPOW	-28		3	dBm
Damage threshold, each lane	RDAM		4		dBm
Receive Power, each lane (OMA)	RxOMA	3			dBm
Receive Sensitivity (OMA), each lane	RxSENS			-28	dBm
Receiver Reflectance	REFLR			-26	dB
LOS Assert, each lane	LOSA	-39			dBm
LOS De-Assert, each lane	LOSD			-29	dBm
LOS Hysteresis, each lane		0.5			dB

Note:

1) Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2) Hit ratio 5x10-5.
3) Receiver sensitivity (OMA), each lane (max) at 5x10-5 BER is a normative specification.

Performance Specifications - Electrical

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Differential data input swing per lane	Vin	300		900	mVp-p	
Input Impedance (Differential)	Zin	90	100	110	%	
Receiver						
Output Amplitude (Differential)	Vout	300		900	mVp-p	
Output Impedance (Differential)	Zout	90	100	110	%	
Output Rise/Fall Time	tr/tf			20	ps	20%~80%

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	+85	°C
Maximum Supply Voltage	VCC	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%

Note:
Exceeding any one of these values may destroy the device immediately.

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Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	Tc	-40		85	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Dissipation	PD			7.5	W

Digital Diagnostic Functions

Parameter	Range	Unit	Accuracy	Calibration
Temperature	-40 to 85	°C	±3°C	Internal / External
Voltage	3.1 to 3.5	V	±3%	Internal / External
Bias Current, each lane	30 to 110	mA	±10%	Internal / External
TX Power, each lane	2 to 6	dBm	±3dB	Internal / External
RX Power, each lane	-28 to 3	dBm	±3dB	Internal / External

Note:

The transceivers provide serial ID memory contents and diagnostic information about the present operating conditions by the 2-wire serial interface (SCL, SDA). The diagnostic information with internal calibration or external calibration all are implemented, including received power monitoring, transmitted power monitoring,
bias current monitoring, supply voltage monitoring and temperature monitoring.

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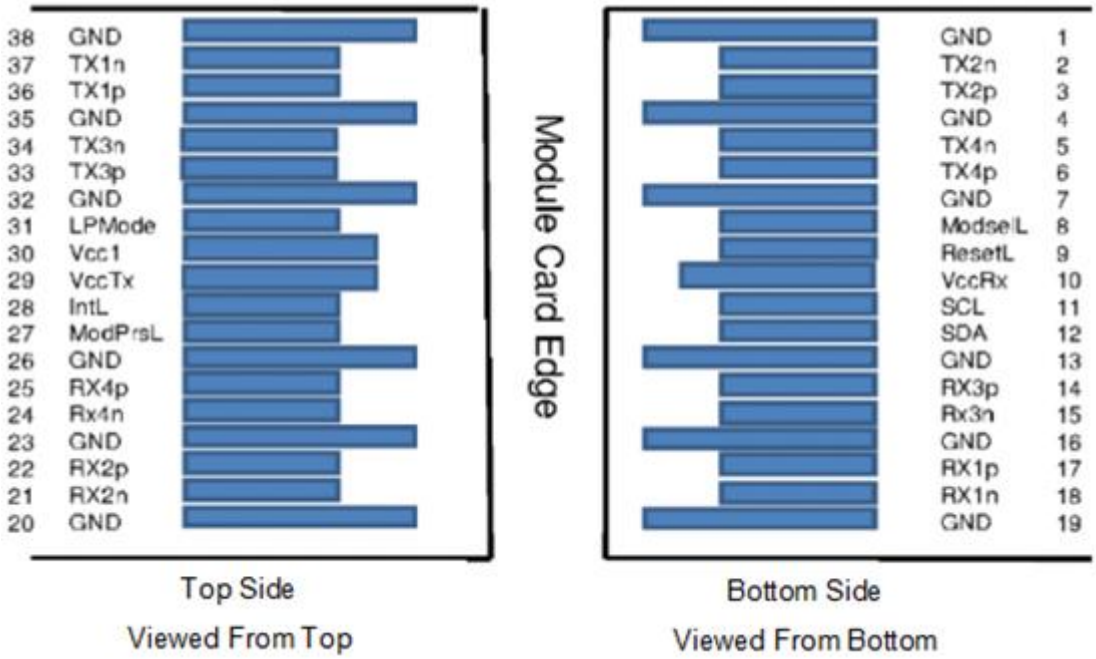
Electrical PIN Pad Layout and Details



Pin Function Definitions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1)
2	CML-1	Tx2n	Transmitter Inverted Data Input	3	
3	CML-1	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1)
5	CML-1	Tx4n	Transmitter Inverted Data Input	3	
6	CML-1	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1)
8	LVTTL-1	ModSelL	Module Select	3	
9	LVTTL-1	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2)
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1)
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1)

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17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1)
20		GND	Ground	1	1)
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1)
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1)
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2)
30		Vcc1	+3.3V Power supply	2	2)
31	LVTTL-1	LPMode	Low Power Mode	3	
32		GND	Ground	1	1)
33	CML-1	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-1	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1)
36	CML-1	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-1	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1)

Notes:

1) GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2) Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1and Vcc Tx may be internally connected within the QSFP28 Module in any combination. The connector pins are each rated for a maximum current of 500Ma.

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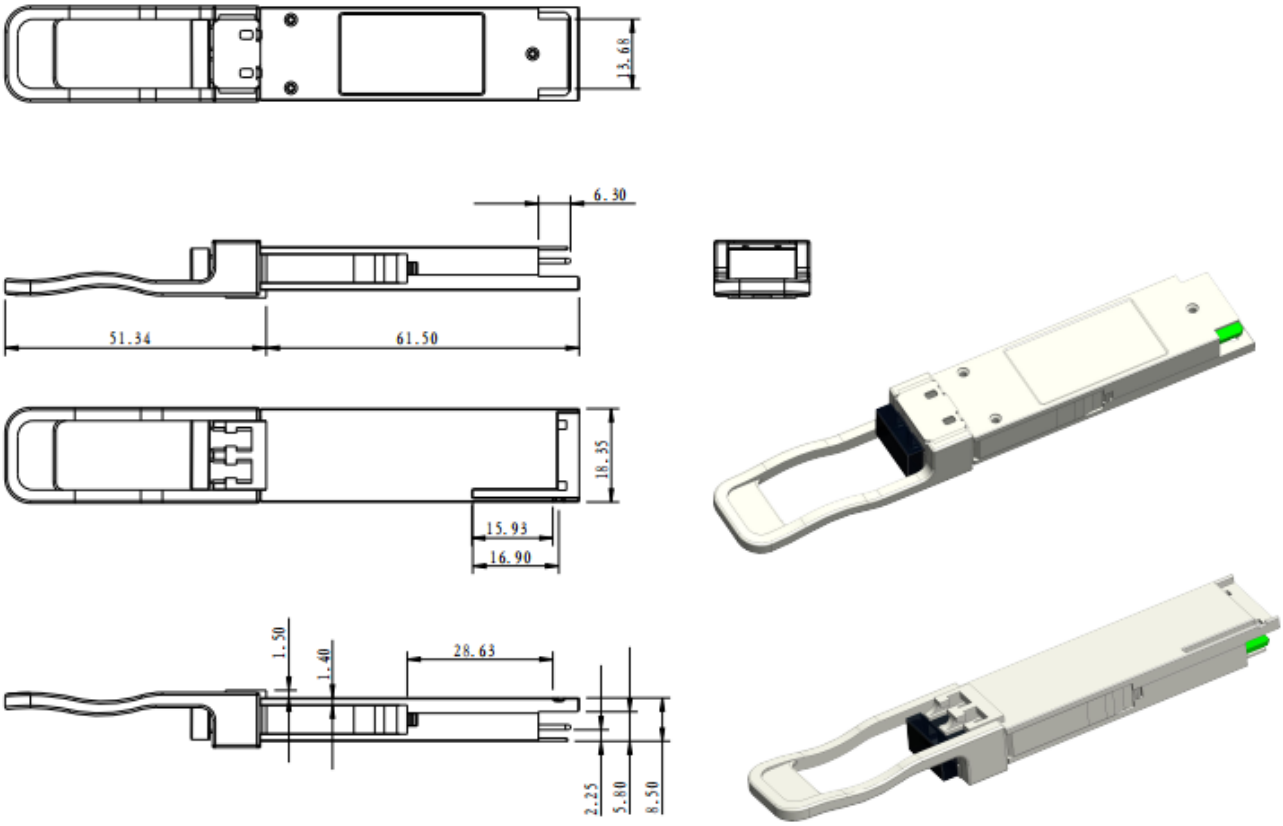
Mechanical Specifications



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Regulatory Compliance

Feature	Standard	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883G Method 3015.7	Class 1C (>1000V)
Electrostatic Discharge (ESD) to the enclosure	EN 55035:2017/A11:2020 IEC-61000-4-2	Compliant with standards
Electromagnetic Interference (EMI)	CFR47, FCC Part 15 Subpart B, ANSI C63.4:2014 EN55032:2015+A11:2020 CISPR 16-2-1	Compliant with standards Noise frequency range: 30MHz to 6GHz. Good system EMI design practice required to achieve Class B margins. System margins are dependent on customer host board and chassis design.
Electromagnetic Immunity	EN 55024: 2010+A1:2015 IEC 61000-4-3	Compliant with standards. 1KHz sine-wave, 80% AM, from 80MHz to 1GHz. No effect on transmitter/receiver performance is detectable between these limits.
RoHS 10	2011/65/EU and the amendment directive (EU) 2015/863	Compliant with standards
Component Recognition	EN 62368-1:2014+A11 EN 60825-1:2014 EN 60825-2:2004+A1+A2	CE No.: CTB220615038E UL file: CN21EFMW 001 TüV Certificate No. R 50491717

Appendix: Document Revision

Version No.	Date	Description
1.0	2021-06-07	For the first time to issue

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