400G QSFP-DD VR4 50m Transceivers
CC-QSFD04VR4-12D

Features

The 400G QSFP-DD VR4 Optical Transceiver offers the following features:

- Support 100GBASE per lane in multimode fiber
- Data rate up to 425Gbps (4x 106.25Gbps)
- Reach up to 50m on MMF(OM4)
- 850nm VCSEL laser and PIN receiver
- High speed I/O electrical interface (400GAUI-8)
- Single MPO-12 receptacle
- Operating case temperature: 0 to +70°C
- Compliant to RoHS 6/6
- Compliant to QSFP-DD MSA and CMIS5.0

Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Units
Case Operating Temperature [1,2]	TOP	0	70	°C
Power Supply Voltage	Vcc	-0.5	3.6	V
Storage Temperature Range [1,2]	TST	-40	85	°C
Operating Relative Humidity [1,2,3]	RH	5	85	%

Notes:
[1] Absolute Maximum Ratings are those beyond which damage to the device may occur.
[2] Between the Recommended Operating conditions and Absolute Maximum ratings,prolonged operation is not intended, and permanent device degradation may occur.
[3] Non-condensing.

Optical Specification(General)

Parameter	400GBASE-VR4
Application code	400G-VR4
Standard	IEEE Std 802.3db&IEEE Std 802.3bs
Data rate(Gb/s)	425Gb/s

Transmitter Optical Characteristics

Parameter		400GBASE-VR4	Unit
Signaling rate, each lane (range)		53.125 ± 100 ppm	GBd
Modulation format		PAM4	-
Center wavelength (range)		842 ~ 948	nm
RMS spectral width[1] (max)		0.65	nm
Average launch power, each lane (max)		4	dBm
Average launch power, each lane (min)		-4.6	
Outer Optical Modulation Amplitude (OMAouter), each lane (max)		3.5	dBm
Outer Optical Modulation Amplitude (OMAouter),each lane (min)	for max(TECQ, TDECQ)≤1.8 dB	–2.6	dBm
	for1.8＜max(TECQ, TDECQ)≤4.4 dB	-4.4+max (TECQ,TDECQ)	dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)		4.4	dB
Transmitter eye closure for PAM4 (TECQ), each lane (max)		4.4	dB

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Overshoot/undershoot (max)	26	%
Transmitter power excursion, each lane (max)	2	dBm
Extinction Ratio	2.5	dB
Transmitter transition time, each lane (max)	17	ps
Average launch power of OFF transmitter, each lane (max)	-30	dBm
RIN12OMA (max)	-131	dB/Hz
Optical return loss tolerance (max)	12	dB
Encircled flux[2]	≥86% at 19 nm	-
	≤30% at 4.5um	

Notes:
[1] RMS spectral width is the standard deviation of the spectrum
[2] If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4

Receiver Optical Characteristics

Parameter		400GBASE-VR4	Unit
Signaling rate, each lane (range)		53.125 ± 100 ppm	GBd
Modulation format		PAM4	-
Center wavelength (range)		842~948	nm
Damage threshold[1] (min)		5	dBm
Average receive power, each lane (max)		4	dBm
Average receive power, each lane[2] (min)		-6.3	dBm
Receive power, each lane (OMAouter) (max)		3.5	dBm
Receiver reflectance (max)		-12	dB
Receiver sensitivity (OMAouter), each lane (max)	for TECQ≤1.8 dB	-4.4	dBm
	for 1.8＜TECQ≤4.4 dB	-6.2+TECQ	dBm
Stressed receiver sensitivity (OMAouter), each lane[3] (max)		-1.8	dBm
Conditions of stressed receiver sensitivity test:[4]			
Stressed eye closure for PAM4 (SECQ), lane under test		4.4	dB
OMAouter of each aggressor lane		3.5	dBm

Notes:
[1] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[2] Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[3] Measured with conformance test signal at TP3 (see 167.8.13) for the BER specified in 167.1.1.
[4] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Transmitter Electrical Characteristics

Parameter	Units	Min	Typ	Max
Signaling rate per lane ± 100 ppm	GBd		26.5625	
Differential peak-to-peak input voltage tolerance	mV	900		
Differential termination mismatch	%			10
Single-ended voltage tolerance range	V	-0.4		3.3
DC common mode voltage	mV	-350		2850

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Receiver Electrical Characteristics

Parameter	Units	Min	Typ	Max
Signaling rate per lane ± 100 ppm	GBd		26.5625	
AC common-mode output voltage RMS	mV			17.5
Differential peak-to-peak output voltage	mV			900
Near-end eye symmetry mask width (ESMW)	ui		0.265	
Near-end eye height, differential	mV	70		
Far-end eye symmetry mask width (ESMW)	ui		0.2	
Far-end eye height, differential	mV	30		
Far-end pre-cursor ISI ratio	%	-4.5		2.5
Differential termination mismatch	%			10
Transition time, 20-80%	ps	9.5		
DC common mode voltage	mV	-350		2850

Electrical Power Supply Characteristics

Parameter	Symbol	Min	Typ.	Max	Units
Power Supply Voltage	V_{CC1} , $V_{CCTx,}$ V_{CCRx}	3.13	3.30	3.47	V
Power Consumption	PW	-	-	7	W
Power Consumption-LP mode	-	-	-	1.5	W

Notes:
The specified characteristics are met within the recommended range of operation. Unless otherwise noted typical data are quoted at nominal voltage and +25°C ambient temperature.

Electrical Pin Definition

Pad	Logic	Symbol	Description	Plug Sequence 4	Notes
1		GND	Ground	1B	1
2	CML - I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML - I	Tx2p	Transmitter Non - Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML - I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML - I	Tx4p	Transmitter Non - Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL - I	ModSelL	Module Select	3B	
9	LVTTL - I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS - I /O	SCL	TWI serial interface clock	3B	
12	LVCMOS - I/O	SDA	TWI serial interface data	3B	
13		GND	Ground	1B	1
14	CML - O	Rx3p	Receiver Non - Inverted Data Output	3B	
15	CML - O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML - O	Rx1p	Receiver Non - Inverted Data Output	3B	

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18	CML - O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML - O	Rx2n	Receiver Inverted Data Output	3B	
22	CML - O	Rx2p	Receiver Non - Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML - O	Rx4n	Receiver Inverted Data Output	3B	
25	CML - O	Rx4p	Receiver Non - Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL - O	ModPrsL	Module Present	3B	
28	LVTTL - O	IntL / RxLOS	Interrupt /optional RxLOS	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL - I	LPMode /TxDis	Low Power mode /optional TX Disable	3B	
32		GND	Ground	1B	1
33	CML - I	Tx3p	Transmitter Non - Inverted Data Input	3B	
34	CML - I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML - I	Tx1p	Transmitter Non - Inverted Data Input	3B	
37	CML - I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML - I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML - I	Tx6p	Transmitter Non - Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML - I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML - I	Tx8p	Transmitter Non - Inverted Data Input	3A	
45		GND	Ground	1A	1
46	LVCMOS/CML - I	P/VS4	Programmable/Module Vendor Specific 4	3A	5
47	LVCMOS/CML - I	P/ VS1	Programmable/Module Vendor Specific 1	3A	5
48		VccRx1	3.3V Power Supply	2A	2
49	LVCMOS/CML - O	P/ VS2	Programmable/Module Vendor Specific 2	3A	5
50	LVCMOS/CML - O	P/ VS3	Programmable/Module Vendor Specific 3	3A	5
51		GND	Ground	1A	1
52	CML - O	Rx7p	Receiver Non - Inverted Data Output	3A	
53	CML - O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML - O	Rx5p	Receiver Non - Inverted Data Output	3A	
56	CML - O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML - O	Rx6n	Receiver Inverted Data Output	3A	
60	CML - O	Rx6p	Receiver Non - Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML - O	Rx8n	Receiver Inverted Data Output	3A	
63	CML - O	Rx8p	Receiver Non - Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2

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69	L VCMOS - I	ePPS /Clock	1PPS PTP clock or reference clock input	3A	6
70		GND	Ground	1A	1
71	CML - I	Tx7p	Transmitter Non - Inverted Data Input	3A	
72	CML - I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML - I	Tx5p	Transmitter Non - Inverted Data Input	3A	
75	CML - I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

Note 1: QSFP - DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP -DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly tothe host board signal - common ground plane. Each connector Gnd contact i s rated for a steady state current of 500mA.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 13 . For po wer classes 4 and above the module differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a steady state current of 1500 mA.

Note 3: Reserved and no Connect pads recommended to be terminated with 10 k W to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2 A, 3A,1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP -DD pads. Sequence 1A and 1B will then occur s imultaneously, followed by 2A and 2B, followed by 3A and 3B.

Note 5 : Full definitions of the P/VS x signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10kΩ .

Note 6 : ePPS/Clock if not used recommended to be terminated with 50 to ground on the host.

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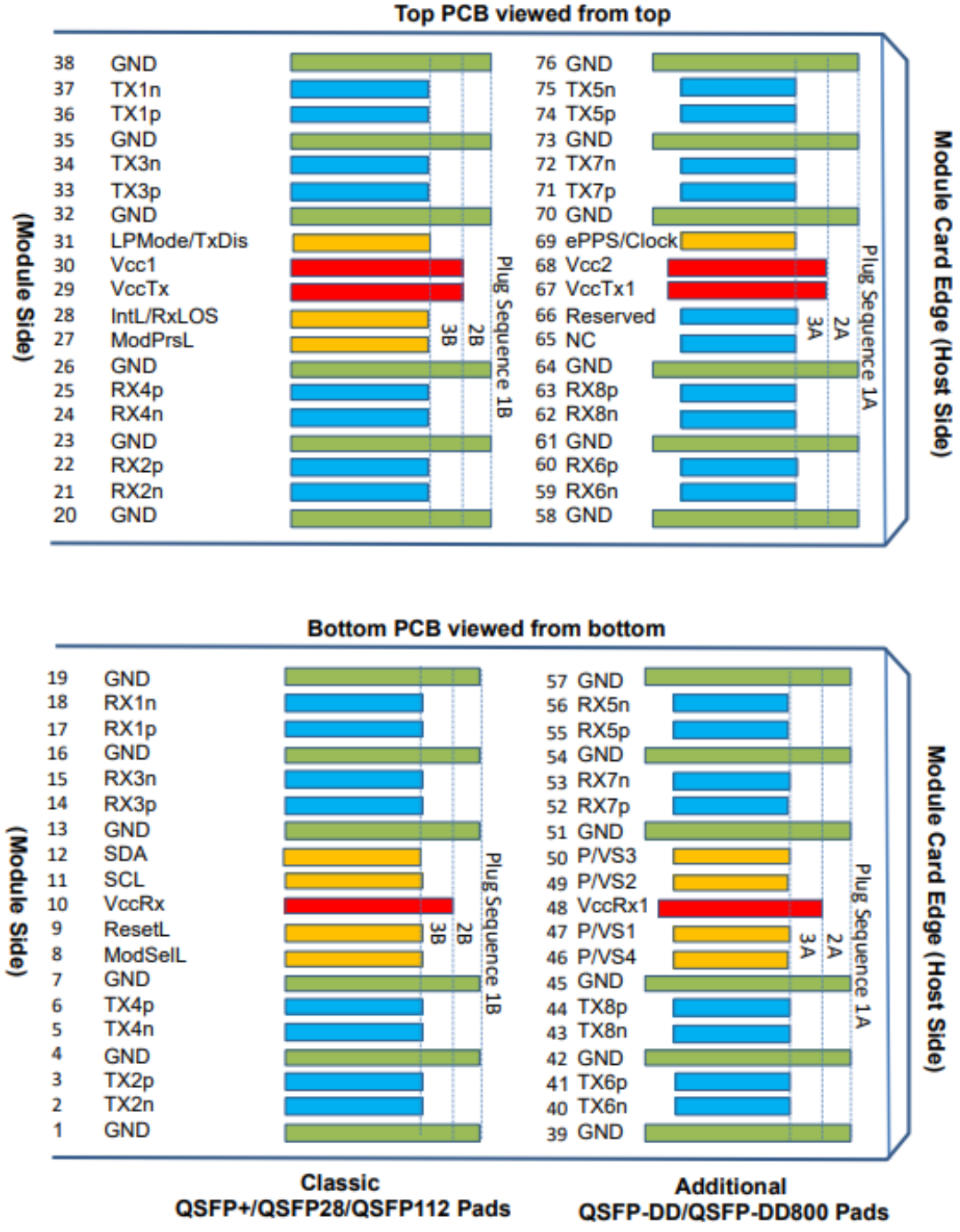
Connector Pad Layout



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Application Notes

Low Speed Electrical Hardware Signals: In addition to the TWI serial interface the module has the following low speed signals for control and status:

- ModSelL
- ResetL
- LPMode/TxDis
- ModPrsL
- IntL/RxLOSL
- P/VS1, P/VS2, P/VS3, and P/VS4.
- ePPS/Clock

ModSelL: The ModSelL is an input signal that shall be pulled to Vcc in the QSFP-DD/QSFP-DD800 modules (see Table 7). When held low by the host, the module responds to TWI serial communication commands. The ModSelL allows the use of multiple QSFP-DD/QSFP-DD800 modules on a single TWI interface bus. When ModSelL is “High”, the module shall not respond to or acknowledge any TWI interface communication from the host.
In order to avoid conflicts, the host system shall not attempt TWI interface communications within the ModSelL de-assert time after any QSFP-DD/QSFP-DD800 modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.
ResetL: The ResetL signal shall be pulled to Vcc in the module (see Table 7). A low level on the ResetL signal for longer than the minimum pulse length (t_Reset_init) (See Table 9) initiates a complete module reset, returning all user module settings to their default state.

Low Speed Electrical Hardware Pins： In addition to the two wire interface (TWI) serial interface the module has the following low speed pins for control and status: a) ModSelL b) LPMode/TxDis c) ResetL d) ModPrsL e) IntL/RxLOS.

LPMode/TxDis:LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the TWI interface except during the execution of a reset. Timing requirements for LPMode/TxDis mode changes are found in, see Table 9. LPMode is used in the control of the module power mode, see CMIS [5] Chapter 6.3.1.3.
When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By using the LPMode signal and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits the host controls how much power a module can consume. When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0. In this mode LPMode/TxDis when set to 1 or 0 disables or enables all optical transmitters within the times specified in Table 9.
Changing LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is high disables all optical transmitters. If the module was in low power mode, then the module transitions out of low power mode at the same time.If the module is already in high power state (Power Override control bits) with transmitters already enabled, the module shall disable all optical transmitters. Changing the LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is low, simply changes the behavior of the mode of LPMode/TxDis. The behavior of the module depends on the Power Override control bits.
Note that the “soft” functions of TxDis, LPMode, IntL and RxLOSL allow the host to poll or set these values over the TWI interface as an alternative to monitoring/setting signal values. Asserting either the “hardware” or “soft bit” (or both) for TxDis or LPMode results in that function being asserted.
Editor’s Note: registers to support optional TxDis will be added in future revisions of CMIS.

ModPrsL: ModPrsL shall be pulled up to Vcc Host on the host board and pulled low in the module (see Table 7). The ModPrsL is asserted “Low” when the module is inserted. The ModPrsL is deasserted “High” when the module is physically absent from the host connector due to the pull-up resistor on the host board.

IntL/RxLOSL: IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled

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up 10 towards Vcc on the host board (see Table 7). At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntL signal is deasserted “High” after all set interrupt flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the TWI interface except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change.
If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane. “high” indicates that there is no loss of received optical power. Timing requirements for IntL/RxLOSL including fast RxLOS mode are found in Table 9. The actual condition of loss of optical receive power is specified by other governing documents, as the alarm threshold level is application specific. The module shall pull RxLOSL to low if any lane in a multiple lane module or cable has a LOS condition and shall release RxLOSL to high only if no lane has a LOS condition.
Programmable/Vendor Specific (Optional):QSFP-DD MSA provides 2 input programmable/vendor specific pads (P/VS1,P/VS4) and 2 output programable/vendor specific pads (P/VS2,P/VS3). Programmable use case also includes vendor proprietary applications. P/VSx I/O are disabled by default.
Editor’s Note - Logic definitions and programmable use cases for P/VSx input/output pads expect to be defined by QSFP-DD HW MSA and CMIS.

ePPS/Clock PTP Reference Clock (Optional): Host ePPS/Clock The ePPS/Clock input is a programable timing and clock input, that can support unmodulated 1PPS (1 pulse per second), modulated (1PPS), and reference clock. The ePPS/clock is a LVCMOS compatible signal with series termination (TBD) on the host board and a parallel termination of at least 4.7 kΩ in the module. To improve signal integrity for faster clocks (i.e., 156.25 MHz) the parallel termination can be reduced to as low as 470 Ω and optionally AC coupled.
For high-performance Precision Time Protocol (PTP) applications, the ePPS (Enhanced Pulse Per Second) reference either with 1PPS modulated or unmodulated may be provided from the host to the module for time synchronization, see Table 2 for advertise capability. This can be used for either offline delay characterization or real-time delay compensation within the module. The ePPS is used to synchronize tightly the Host Time-of-Day counter to the module internal Time-of-Day Counter.
The ePPS/Clock module input optionally can be configured to provide reference clock to the CDR/DSP, see Table 2 for advertise capability.

Digital Diagnostic Specification

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-3%		+3%	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-3		+3	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-3		+3	dB	Per channel

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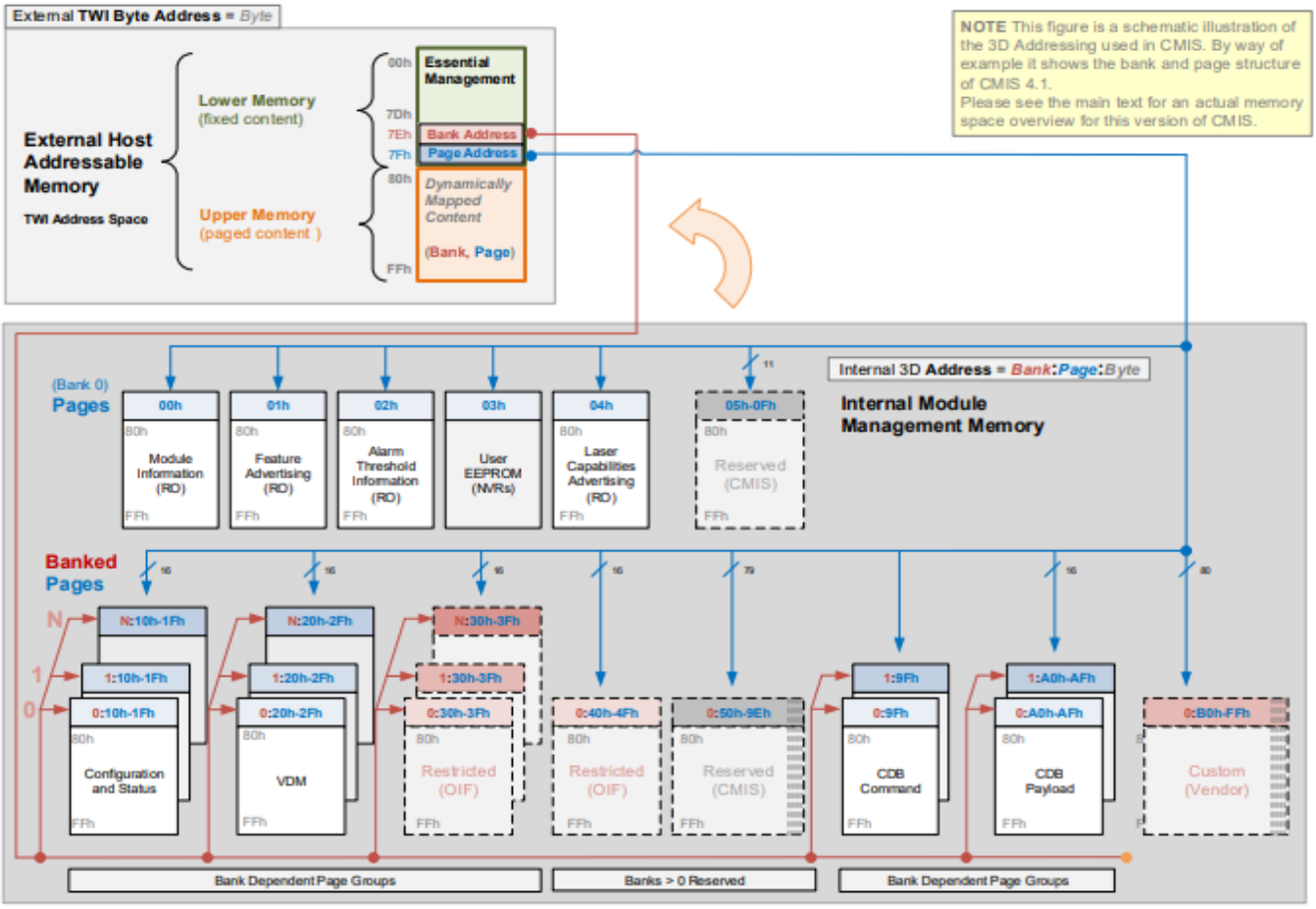
Memory Map



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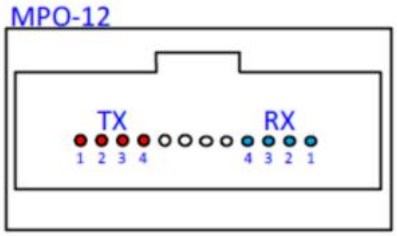
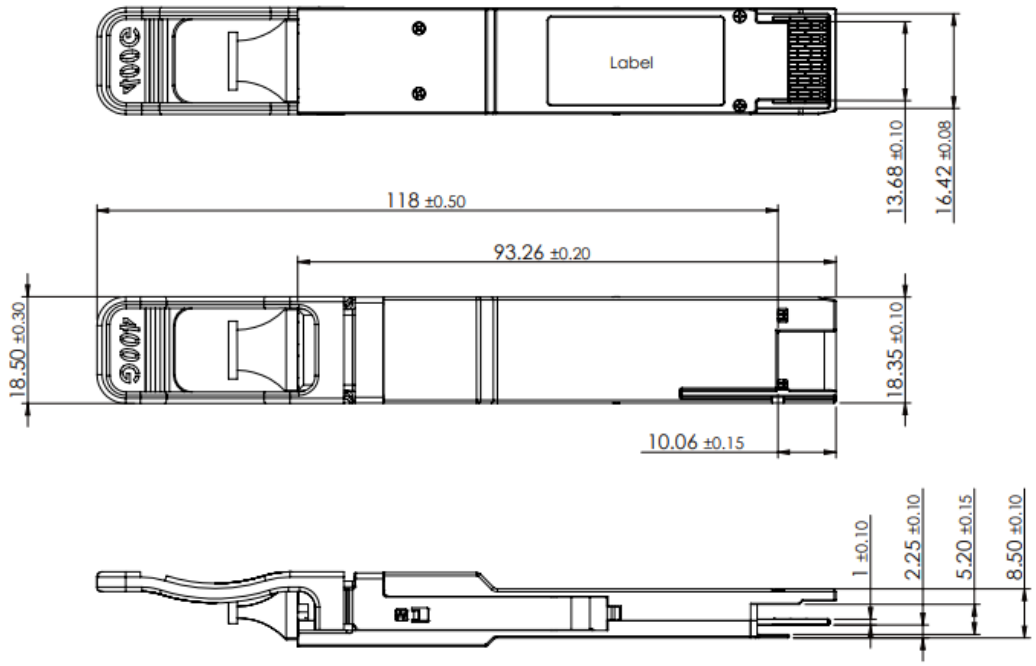
OPTICAL INTERFACE LANES AND ASSIGNMENT

The recommended location and numbering of the optical ports for 3 Media Dependent Interfaces (MDI) are shown as below. The transmit and receive optical lanes shall occupy the positions depicted when looking into the MDI receptacle with the connector keyway feature on top.



Optical media dependent interface port assignment

Mechanical Specifications



Notes:
All dimensions shown are in millimetres.
Tolerances are in accordance with QSFP-DD MSA.

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Ordering Information

Crealights PN	Operating Temperature	Wavelength	Reach	Latch Color
CC-QSFD04VR4-12D	0°C to 70°C	850nm	50m	Beige

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