400G DR4 QSFP-DD Transceiver
CC-QSFD04DR4-12D

Features

- Aggregation Mode
  - 400GBASE-DR4 compliant 4x 53.125GBd PAM4
  - 400GAUI-8 compliant 8x 26.5625 GBd PAM4
- Breakout Mode
  - 4x 100GBASE-DR compliant 53.125GBd PAM4
  - 100GAUI-2 compliant 2x 26.5625 GBd PAM4
- QSFP-DD MSA compliant
- MPO-12 connector with 8° angled end-face
- Power consumption <8 W (Target)
- Operating case temperature 0 to 70 ºC
- CMIS 4.0 management interface

Description

CC-QSFD04DR4-12D-MF000, 400GBASE-DR4, hot pluggable optical transceiver is a high-performance solution for 400GE links for up to 500 m over single mode fiber (SMF) with MPO-12 connector. It combines 8x 26.5625 GBd PAM4 electrical lanes into 4x 53.125 GBd PAM4 optical channels in compliance with IEEE 400GBASE-DR4. Superior performance and reliability is achieved through YSOD's advanced transmitter and receiver design using cooled 4x EA-DFB-LDs and 4x PIN PDs.

Applications

- Data Center 400GE 500 m SMF links
- 400GE to 4x 100GE breakout over 500 m
- Switch/Router interconnections

General Description

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Specifications within in this document are subject to change without notice. August 27, 2023

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FUNCTIONAL DESCRIPTION

CC-QSFD04DR4-12D is a fully integrated, 425 Gb/s optical transceiver for SMF links up to 500 m. CC-QSFD04DR4-12D transmits data in compliance with the optical interface specification IEEE Std 802.3-2022 Section 8 400GBASE-DR4. 400GBASE-DR4 specifies the use of 4-level pulse amplitude modulation (PAM4) at 53.125 Gbaud operating at four parallel channels with wavelength on the range of 1304.5-1317.5 nm from four cooled EA-DFB-LDs. The bit rate per lane is 106.25 Gb/s, which produces an aggregate data rate of 425 Gb/s by means PSM to the transmit ports of the MPO-12 connector. The received optical lanes are paralleled from the receive MPO-12 connector ports to 4 PIN-PDs with transimpedance amplifiers (TIAs) to recover the PAM4 for interfacing with the electrical interface.

The electrical interface is in compliance with 400GAUI-8 specified in IEEE Std 802.3-2022 Section 8. 400GAUI-8 specifies the use of eight differential electrical lanes operating at 26.5625 GBd PAM4 per lane. The bit rate per lane is 53.125 Gb/s, resulting in an aggregate data rate of 425 Gb/s that matches the optical line interface. An internal gear box in DSP converts between the eight lanes of the host interface and the four lanes of the line interface.

In addition, by selecting Breakout Mode, CC-QSFD04DR4-12D is complied with the optical interface specification IEEE Std 802.3-2022 Section 8 100GBASE-DR per lane and the electrical interface specification IEEE Std 802.3-2022 Section 8 100GAUI-2 pre two lanes. 100GBASE-DR specifies the use of PAM4 at 53.125 Gbaud and the bit rate per lane is 106.25 Gb/s. 100GAUI-2 specifies the use of PAM4 at 26.5625 Gbaud and the bit rate per lane is 53.125 Gb/s. By means of a 2:1 mux/demux in DSP, 100GBASE-DR optical interface is connected to 100GAUI-2 electrical interface.

The bit error ratio (BER) of the optical interface is required by 400GBASE-R (Aggregation Mode) and 100GBASE-R (Breakout Mode) to be less than 2.4 x 10-4. The host side shall have Forward Error Correction (FEC) capability based on RS(544,514) requirements defined by IEEE Std 802.3-2022 Section 8 to meet the frame loss ratio requirements of 400GE and 4x 100GE.

The form factor of CC-QSFD04DR4-12D is QSFP56-DD Type 2A and is compliant with the hardware and Common Management Interface Specifications (MIS) of the QSFP-DD multi-source agreement (MSA). QSFP-DD modules can support up to eight electrical lanes on the host interface, which is double the number of lanes supported by QSFP28 or QSFP+ modules. The unique feature of QSFP-DD ports is that they are mechanically and electrically compatible with QSFP28 and QSFP+. Hence, the same port can be used to support multiple generations of modules and data rates if the networking hardware is designed for such operation.

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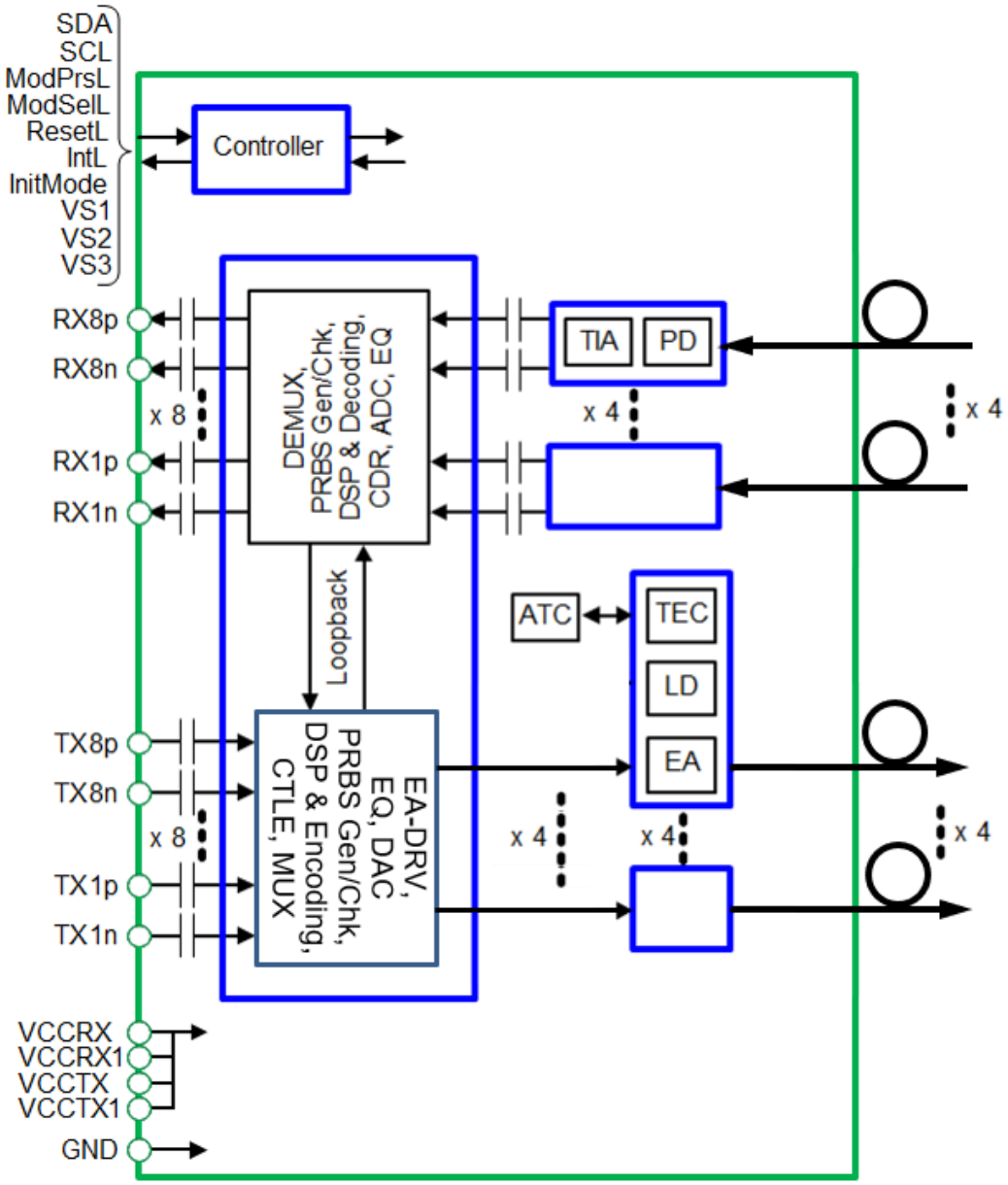

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Absolute Maximum Ratings

No.	Parameter	Symbol	Min.	Max.	Unit	Remarks
1	Supply Voltage	Vcc	0	+3.6	V	
2	Storage Temperature		-40	85	°C	
3	Optical Receiver Input		-	+5.4	dBm	Average, each lane

Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

No	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Supply Voltage	Vcc	3.135	3.3	3.465	V	
2	Supply Voltage Noise Tolerance	PSNR	-	-	66	mV	10 Hz –10 MHz
3	Power Consumption	P_4	-	-	8	W	Targer
4	Instantaneous peak current	Icc_ip_4			3200	mA	
5	Sustained peak current	Icc-sp_4			2640.3	mA	
6	Supply Current	Icc-4	--	-	2551.8	mA	Steady state
7	Case Temperature	TC	0	25	70	°C	

Electrical Characteristics

No.	Parameter	Min.	Typ.	Max.	Unit	Remarks
Module output (each lane, at TP4) [Note 1]						
1	Signaling rate per lane (range)	26.5625-100ppm	26.5625	26.5625+100ppm	GBd	
2	AC Common-mode output voltage (RMS)	-	-	17.5	mV	
3	Differential peak-to-peak output voltage	-	-	900	mV	
4	Near-end ESMW (Eye symmetry mask width)	0.265	-	-	UI	
5	Near-end Eye height, differential	70			mV	
6	Far-end ESMW (Eye symmetry mask width)	0.2	-	-	UI	
7	Far-end Eye height, differential	30	-	-	mV	
8	Far-end pre-cursor ISI ratio	-4.5	-	2.5	%	
9	Differential output return loss	Equation (83E-2)	-	-	dB	Note 2
10	Common to differential mode conversion return loss	Equation (83E-3)	-	-	dB	Note 2
11	Differential termination mismatch	-	-	10	%	
12	Transition time (20% to 80%)	9.5	-	-	ps	
13	DC common mode voltage	-350	-	2850	mV	

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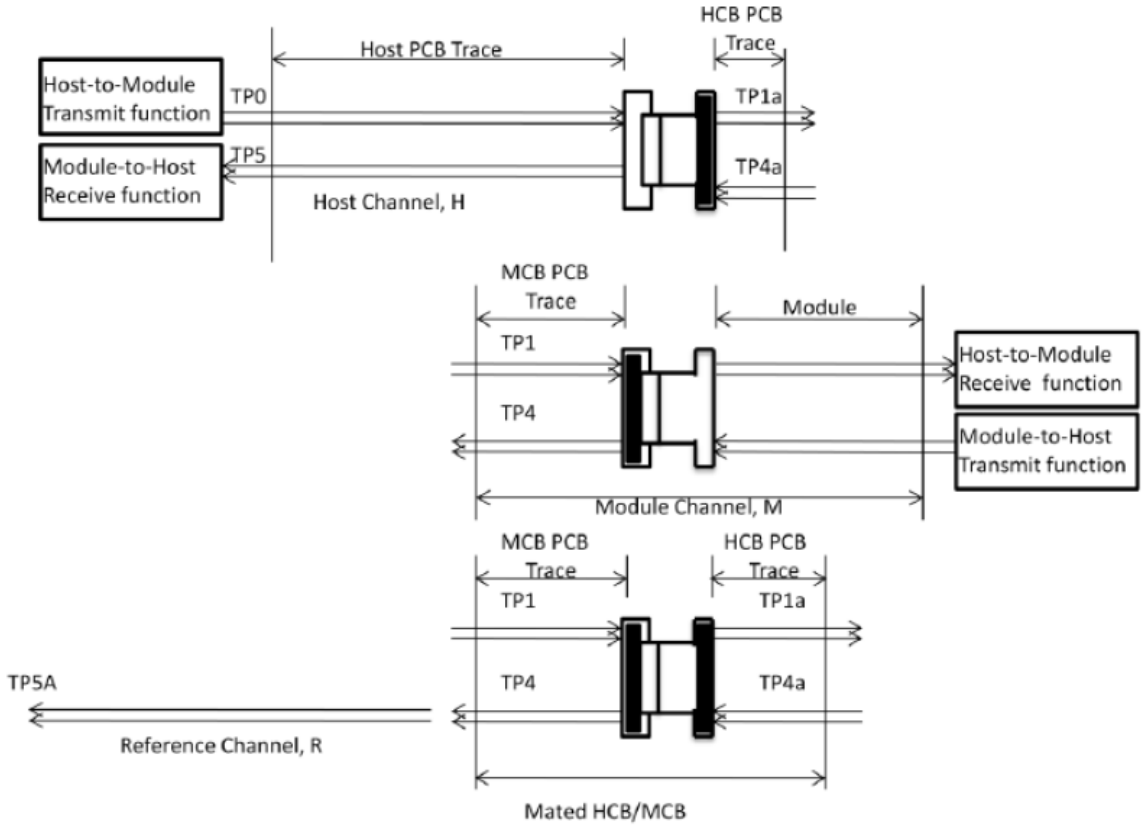
Module input (each lane)						
1	Signaling rate per lane (range)	26.5625-100ppm	26.5625	26.5625+100ppm	GBd	
2	Differential pk-pk input voltage tolerance	900	-	-	mV	at TP1a
3	Differential input return loss	Equation (83E-5)	-	-	dB	at TP1, Note 2
4	Differential to common mode input return loss	Equation (83E-6)	-	-	dB	at TP1, Note 2
5	Differential termination mismatch	-	-	10	%	at TP1
6	ESMW (Eye symmetry mask width)	0.22	-	-	UI	at TP1a
7	Eye width	0.22	-	-	UI	at TP1a
8	Applied pk-pk sinusoidal jitter	Table 120E–6			MHz, UI	at TP1a
9	Eye height	32	-	-	mV	at TP1a
10	Single-ended input voltage tolerance range	-0.4	-	3.3	V	at TP1a
11	DC common mode voltage	-350	-	2850	mV	at TP1

Note 1: Electrical module output is squelched for loss of optical input signal.
Note2: IEEE Std 802.3-2022 Section 6



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Optical Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Channel data rate	f_{DC}		106.25		Gb/s	
2	Signaling rate	f_{SG}		53.125		GBd	PAM4
3	Signal speed variation from nominal	$\triangle f_{SG}$	-100		+100	ppm	
4	Lane wavelength (range)	λ_C	1304.5		1317.5	nm	
5	Side-mode suppression ratio	SMSR	30			dB	
6	Average launch power, each lane		-2.9		4.0	dBm	Note 1
7	Outer Optical Modulation Amplitude (OMAouter), each lane		-0.8		4.2	dBm	Note 2
8	Launch power in OMAouter minus TDECQ, each lane		-2.2			dBm	
9	Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.4	dB	
10	Average Optical Output Power of Off Transmitter, each lane	Poff			-15	dBm	
11	Extinction Ratio, each lane	ER	3.5			dB	
12	RIN21.4OMA				-136	dB/Hz	
13	Optical return loss tolerance				21.4	dB	
14	Transmitter reflectance				-26	dB	Note 3
15	Average receive power, each lane		–5.9		4.0	dBm	Note 4
16	Receive power (OMAouter), each lane				4.2	dBm	
17	Receiver reflectance				-26	dB	
18	Receiver sensitivity (OMAouter), each lane		Max (-3.9, SECQ -5.3),			dBm	Note 5, 6
19	Stressed receiver sensitivity (OMAouter), each lane				-1.9	dBm	Note 5, 7
Conditions of stressed receiver sensitivity test [Note 8]							
20	Stressed eye closure for PAM4 (SECQ), lane under test	SECQ		3.4		dB	
21	OMAouter of each aggressor lane			4.2		dBm	

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
Note 2: Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed these values.
Note 3: Transmitter reflectance is defined looking into the transmitter.
Note 4: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
Note 5: For when Pre-FEC BER is 2.4 x 10-4.
Note 6: Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.
Note 7: Measured with conformance test signal at TP3 for the BER specified in IEEE Std 802.3-2022 124.1.1.
Note 8: These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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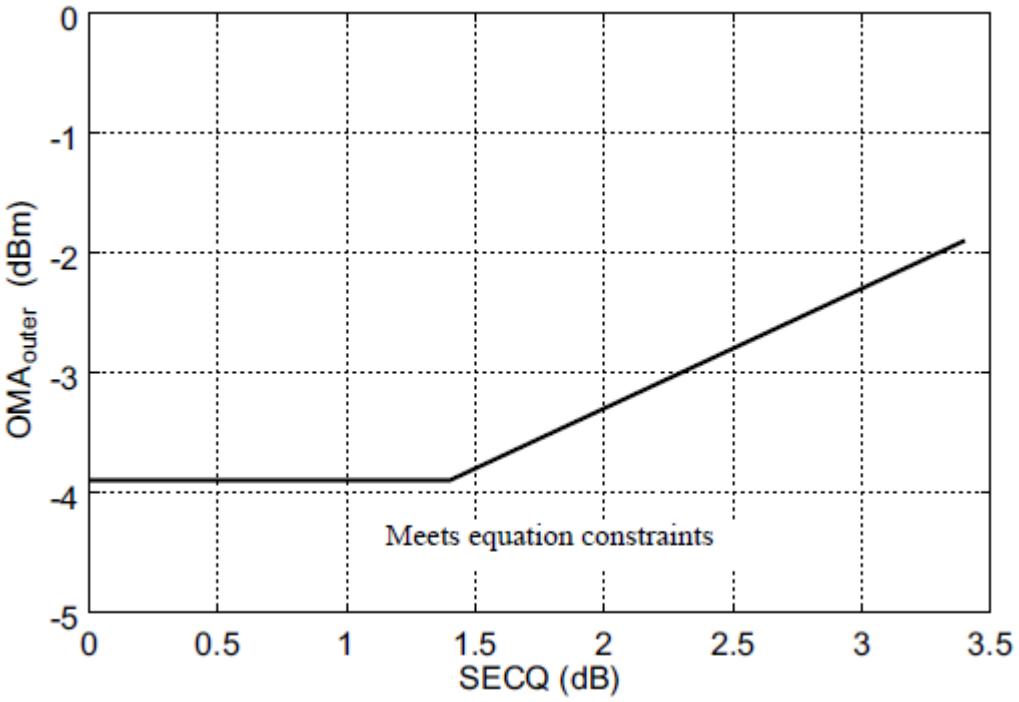

RX_LOS Characteristics

No.	Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
1	Receiver Loss of Signal Indicator Assert Level	RX_LOS	-15	-	-7.9	dBm	Average power
2	Receiver Loss of Signal Indicator De-assert Level		-	-	-7.4	dBm	Average power
3	Hysteresis		0.5			dB	

Rx(n)(p/n)

Rx(n)(p/n) are QSFP-DD module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC. The QSFP-DD module host interface is internally AC coupled, so AC-coupling is not required on the host PCB.
Output squelch for loss of optical input signal (RX Squelch) is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output. In the squelched state, output impedance levels are maintained, while the differential voltage amplitude shall be less than 50 mVpp.

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Tx(n)(p/n)

Tx(n)(p/n) are QSFP-DD module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP-DD optical module. The AC coupling is implemented inside the QSFP-DD optical module and not required on the Host board.
Output squelch for loss of electrical signal (Tx Squelch) is an optional function. Where implemented, it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 150 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel, the loss of any of the incoming electrical input channels causes the optical output channel to be squelched.
For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

Low Speed Control Pins

In addition to the 2-wire serial interface the transceiver has the following low speed signals for control and status: LPMode, ResetL, ModSel, IntL and ModPrsL. See the QSFP-DD MSA Hardware Specification for detailed descriptions of each signal.

Low Speed Electrical Specifications

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc.

Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL (max)=3 mA for fast mode, 20 mA for Fast-mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use 3 kohm pullup resistor, max. For 1000 kHz clock rate refer to Figure 6 in QSFPDD MSA HW Spec [3].
	Cb		200	pF	For 400 kHz clock rate use 1.6 kohm pullup resistor, max. For 1000 kHz clock rate refer to Figure 6 in QSFPDD MSA HW Spec [3].
LPMode, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
	|Iin|		360	uA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0 mA
	VOH	Vcc-0.5	Vcc+0.3	V	10 kohm pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL= 2.0mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

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2-Wire Management Interface

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. This QSFP-DD specification is based on SFF-8636 but with modifications to support an 8-channel module, and as such is not directly backwards compatible with SFF-8636. Byte 00 on the Lower Page or Address 128 Page 00 is used to indicate the use of the QSFP-DD memory map rather than the QSFP memory map.

The QSFP-DD Module supports alarm, control and monitor functions via a two-wire interface bus. Upon module initialization, these functions are available. QSFP-DD two-wire electrical interface consists of 2 pins of SCL (2-wire serial interface clock) and SDA (2-wire serial interface data). The low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. The timing requirements on the two-wire interface are listed in Table 7 and Figure 4.

Management Interface Timing

Parameter	Symbol	Fast Mode Plus (1MHz)		Unit	Conditions
		Min	Max		
Clock Frequency	fSCL	0	1000	kHz	
Clock Pulse Width Low	tLOW	0.50		μs	
Clock Pulse Width High	tHIGH	0.26		μs	
Time bus free before new transmission can start	tBUF	1		μs	Between STOP and START and between ACK andReStart
START Hold Time	tHD.STA	0.26		μs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.26		μs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		μs	
Data In Setup Time	tSU.DAT	0.1		μs	
Input Rise Time	tR		120	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc), see Figure 6 in QSFPDD MSA HW Spec [3].
Input Fall Time	tF		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc), in QSFPDD MSA HW Spec [3]
STOP Setup Time	tSU.STO	0.26		μs	
STOP Hold Time	tHD.STO	0.26		us	
Aborted sequence bus release	Deselect _Abort		2	ms	Delay from a host deasserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time1	tSU.ModSelL	2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host initiated serial bus sequence.

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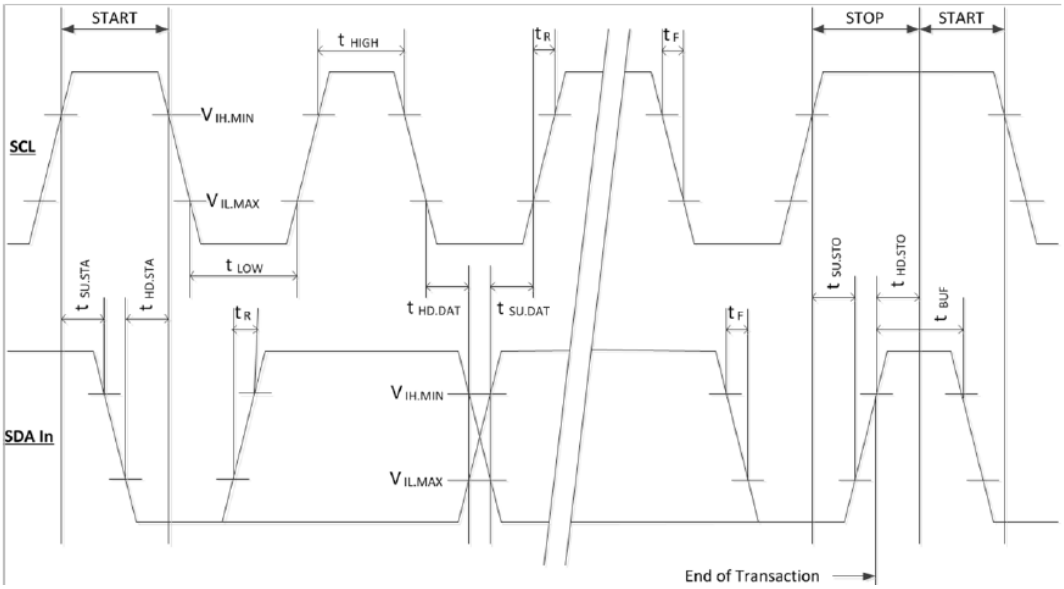
ModSelL Hold Time1	tHD.ModSelL	2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module select status.
Serial Interface Clock Holdoff “Clock Stretching”	T_clock_hold		500	us	Time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation.
Complete Single or Sequential Write to non-volatile registers	tWR		80	ms	Time to complete a Single or Sequential Write to non-volatile registers.
Accept a single or sequential write to volatile memory.	tNACK		10	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC		10	ms	Time to complete a memory bank and/or page change.
Endurance (Write Cycles)		50k		cycles	Module Case Temperature= 70 °C

Note 1: When the host has determined that module is QSFP-DD, the management registers can be read to determine alternate supported ModSelL set up and hold times.



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Soft Control and Status Functions

Table 8 lists the required timing performance for software control and status functions.

Control and Status Timing Requirements

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on1, hot plug or rising edge of reset until until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction.
ResetL Assert Time	t_reset_init	10		μs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
IntL Deassert Time	toff_IntL		500	μs	Time from clear on read2 operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)3 until associated IntL assertion is inhibited.
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)3 until associated IntL operation resumes.

Note 1: Power on is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 2.
Note 2: Measured from the rising edge of SDA in the stop bit of the read transaction.
Note 3: Measured from the rising edge of SDA in the stop bit of the write transaction.
Note 4: Rx LOS condition is defined at the optical input by the relevant standard.

POWER

The power supply has six designated pins, VccTx, VccTx1, Vcc1, Vcc2, VccRx, VccRx1 in the connector. Vcc1 and Vcc2 are used to supplement VccTx, VccTx1, VccRx or VccRx1 at the discretion of the module vendor. Power is applied concurrently to these pins.
A host board together with the QSFP-DD module(s) forms an integrated power system. The host supplies

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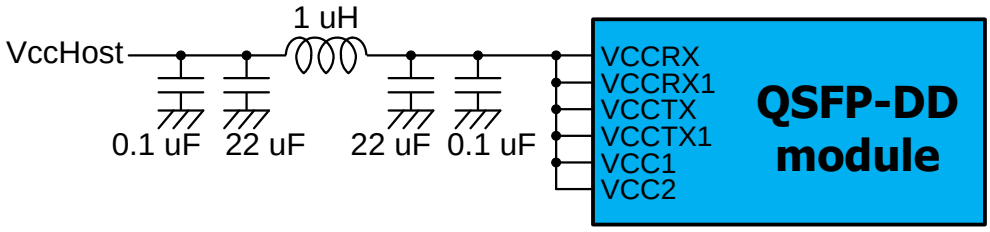
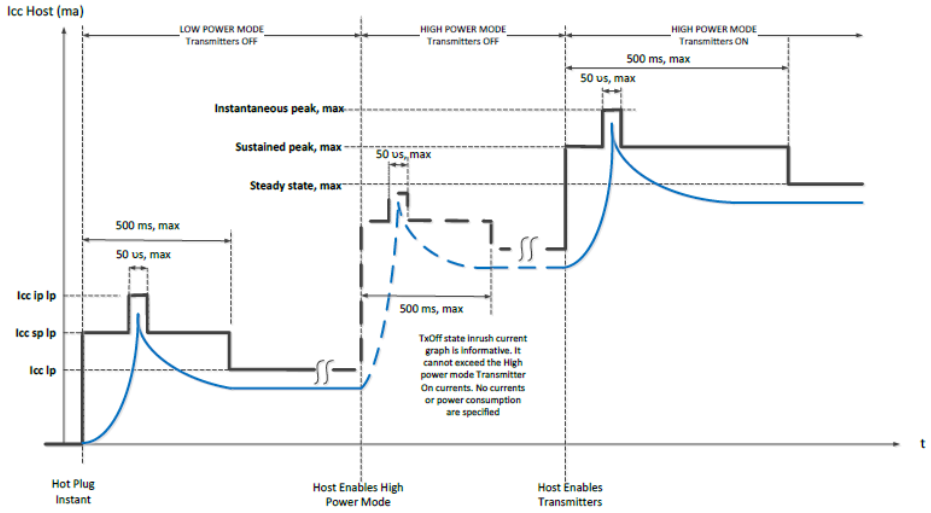
stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.
All power supply requirements in Table 2 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.
QSFP56-DD modules are categorized into several power classes as listed in Table 10. The power class of CC-QSFD04DR4-12D is class 4.

Power Class	Max Power (W)
1	1.5
2	3.5
3	7.0
4	8.0
5	10
6	12
7	14
8	>14

Host Board Power Supply Filtering



Module Power Supply Specification



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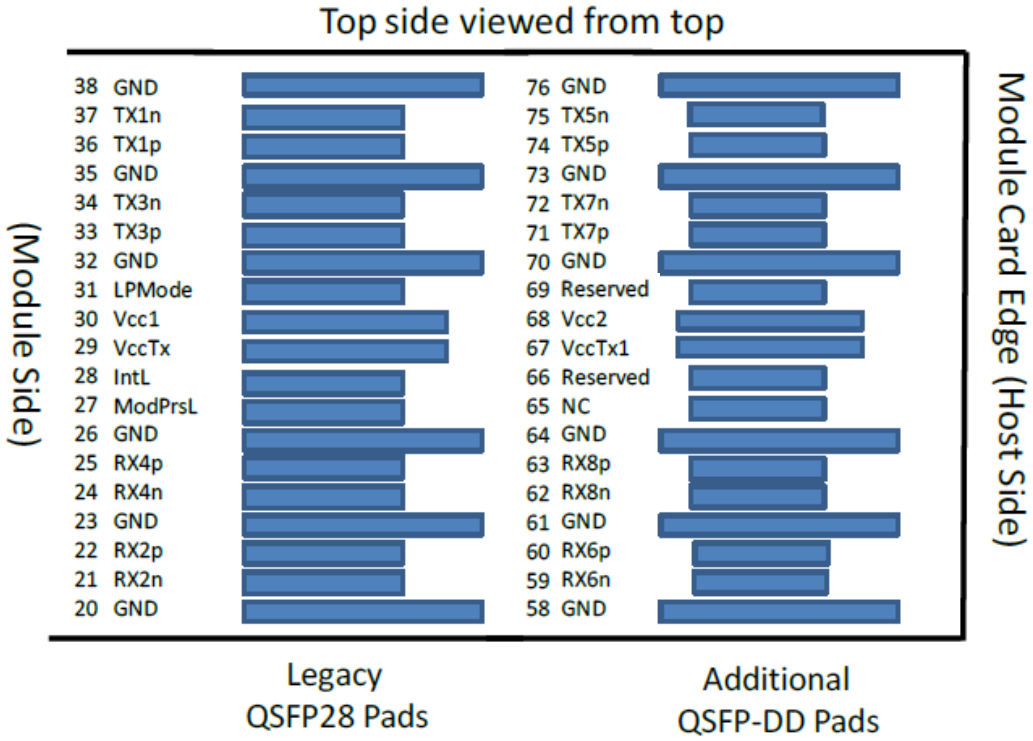
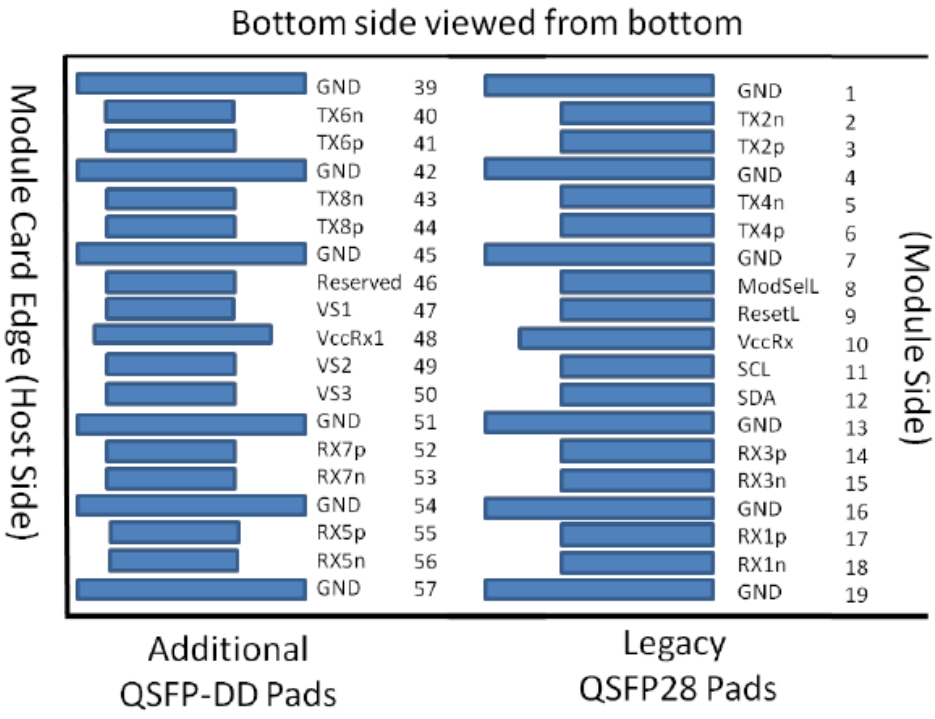
PIN ASSIGNMENT





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Pin Description

Pad	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data	3B	
34	CML-I	Tx3n	Transmitter Inverted Data	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data	3B	
37	CML-I	Tx1n	Transmitter Inverted Data	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2

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49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol(PTP)	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data	3A	
72	CML-I	Tx7n	Transmitter Inverted Data	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data	3A	
75	CML-I	Tx5n	Transmitter Inverted Data	3A	
76		GND	Ground	1A	1

Notes:

1.QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2.VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently.Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated.

3.All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10kohms and less than 100pF.

4.Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads.Sequence 1A,1B will then occur simultaneously, followed by 2A,2B,followed by 3A,3B

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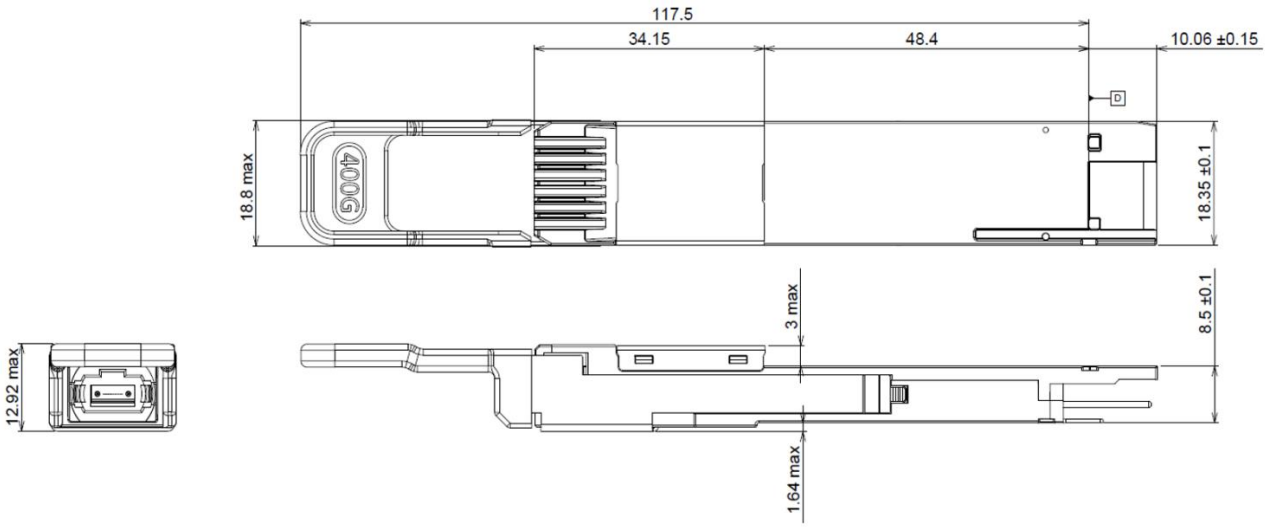
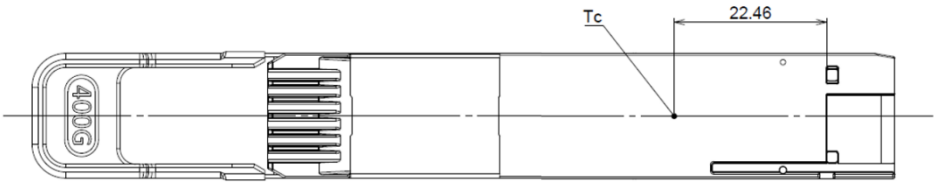
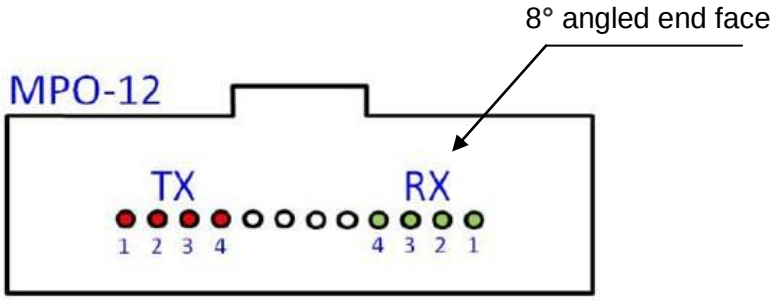
MECHANICAL DIMENSIONS







Looking into the connector, transmitter is on the left.

Appendix A Document Revision

Version No.	Date	Description
V1.0	2024-03-20	First released

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