400G QSFP112 100m SR4 Transceivers
CC-QCS110M-SD

1.1 General Description

This module is a hot pluggable fiber optic transceiver in the QSFP form factor with digital diagnostics monitoring functionality (DDM) and control function. The 400G QSFP112 SR4 module has four identical and independent lanes which provides a point-to-point 400Gb/s link over OM4 multimode fiber up to 100m. This makes it an ideal low-cost solution for short reach data center optical interconnects.

The central wavelength of each lane is at 850nm wavelength. The low power consumption and excellent EMI performance enable system design with high port density. The product is designed and tested in accordance with industry safety standards. The transceiver is Class 1 Laser product per U.S. FDA/CDRH and IEC 60825-1:2007 & IEC 60825-2:2004+A1+A2standards.

The transceiver can be conveniently assembled into and released from the host system through the latch.

The transceiver operates from a single +3.3V power supply over an operating case temperature range of 0°C to +70°C. The housing is made of metal for EMI immunity.

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1.2 Features

The 400G QSFP112 SR4 Optical Transceiver offers the following features:

- Support 100GBASE per lane in multimode fiber
- Hot-pluggable QSFP112 Type 1 form factor
- Data rate up to 425Gbps (4x 106.25Gbps)
- Reach up to 100m on MMF(OM4)
- 850nm VCSEL laser and PIN receiver
- High speed I/O electrical interface (400GAUI-4)
- Single MPO-12 receptacle
- Operating case temperature: 0 to +70°C
- Compliant to RoHS 6/6
- Compliant to 400G QSFP112 MSA and CMIS4.0

1.3 Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Units
Case Operating Temperature [1,2]	T_{OP}	0	70	°C
Power Supply Voltage	*Vcc*	-0.5	3.6	V
Storage Temperature Range [1,2]	T_{ST}	-40	85	°C
Operating Relative Humidity [1,2,3]	*RH*	5	85	%

Notes:
[1] Absolute Maximum Ratings are those beyond which damage to the device may occur.
[2] Between the Recommended Operating conditions and Absolute Maximum ratings, prolonged operation is not intended, and permanent device degradation may occur.
[3] Non-condensing.

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2 Product Specification

2.1 Optical Specification(General)

Parameter	400GBASE-SR4
Application code	400G-SR4
Standard	IEEE Std 802.3db&IEEE Std 802.3ck
Data rate(Gb/s)	425Gb/s

2.2 Transmitter Optical Characteristics

Parameter	400GBASE-SR4	Unit
Signaling rate, each lane (range)	53.125 ± 100 ppm	GBd
Modulation format	PAM4	-
Center wavelength (range)	844~863	nm
RMS spectral width[1] (max)	0.6	nm
Average launch power, each lane (max)	4	dBm
Average launch power, each lane (min)	-4.6	
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (max)	3.5	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane (min) for max(TECQ, TDECQ)≤1.8 dB or 1.8<max(TECQ, TDECQ)≤4.4 dB	 −2.6 -4.4+max (TECQ,TDECQ)	 dBm dBm
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane (max)	4.4	dB
Transmitter eye closure for PAM4 (TECQ), each lane (max)	4.4	dB
Overshoot/undershoot (max)	26	%
Transmitter power excursion, each lane (max)	2	dBm
Extinction Ratio	2.5	dB
Transmitter transition time, each lane (max)	17	ps
Average launch power of OFF transmitter, each lane (max)	-30	dBm
$RIN_{12}OMA$ (max)	-131	dB/Hz
Optical return loss tolerance (max)	12	dB
Encircled flux[2]	⩾86% at 19 nm ⩽30% at 4.5um	-

Notes:
[1] RMS spectral width is the standard deviation of the spectrum
[2] If measured into type A1a.2 or type A1a.3, or A1a.4, 50 μm fiber, in accordance with IEC 61280-1-4

2.3 Receiver Optical Characteristics

Parameter	400GBASE-SR4	Unit
Signaling rate, each lane (range)	53.125 ± 100 ppm	GBd
Modulation format	PAM4	-
Center wavelength (range)	842~948	nm
Damage threshold[1] (min)	5	dBm
Average receive power, each lane (max)	4	dBm
Average receive power, each lane[2] (min)	-6.4	dBm
Receive power, each lane (OMA_{outer}) (max)	3.5	dBm
Receiver reflectance (max)	-12	dB
Receiver sensitivity (OMA_{outer}), each lane (max) for TECQ≤1.8 dB for 1.8<TECQ≤4.4 dB	 -4.6 -6.4+TECQ	 dBm dBm
Stressed receiver sensitivity (OMA_{outer}), each lane[3] (max)	-2	dBm
Conditions of stressed receiver sensitivity test:[4]		
Stressed eye closure for PAM4 (SECQ), lane under test	4.4	dB
OMA_{outer} of each aggressor lane	3.5	dBm

Notes:
[1] The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level on one lane. The receiver does not have to operate correctly at this input power.
[2] Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
[3] Measured with conformance test signal at TP3 (see 167.8.13) for the BER specified in 167.1.1.
[4] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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2.4 Transmitter Electrical Characteristics

Parameter	Reference	Value	Unit
Signaling rate, each lane (range)	120G.3.4.1	53.125 ± 50 ppm	GBd
Differential pk-pk input voltage tolerance (min)	120G.5.1	900	mV
Differential to common-mode return loss (min)	120G.3.3.2	Equation (120G-2)	dB
Effective return loss, ERL (min)	120G.3.4.3	8.5	dB
Differential termination mismatch (max)	120G.3.1.3	10	%
Module stressed input test[1]	120G.3.4.2	See 120G.3.4.2	
Single-ended voltage tolerance range (min)	120G.5.1	-0.4 to 3.3	V
DC common-mode voltage (min)[2]	120G.5.1	-350	mV
DC common-mode voltage (max)[2]	120G.5.1	2850	mV

Notes:
[1] Meets BER specified in 120G.1.1.
[2] DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.

2.5 Receiver Electrical Characteristics

Parameter	Reference	Value	Unit
Signaling rate, each lane (nominal)		53.1251	GBd
AC common-mode output voltage (max, RMS)	120G.5.1	17.5	mV
Differential peak-to-peak output voltage (max) Short mode Long mode	120G.5.1	 600 900	 mV mv
Eye height (min)	120G.3.2.2	15	mV
Vertical eye closure, VEC (max)	120G.3.2.2	12	dB
Common-mode to differential return loss (min)	120G.3.1.1	Equation (120G-1)	dB
Effective return loss, ERL (min)	120G.3.2.3	8.5	dB
Differential termination mismatch (max)	120G.3.1.3	10	%
Transition time (min)	120G.3.1.4	8.5	ps
DC common-mode voltage (min)[2]	120G.5.1	-350	mV
DC common-mode voltage (max)[1]	120G.5.1	2850	mV

Notes:
[1] The signaling rate range is derived from the PMD receiver input.
[2] DC common-mode voltage is generated by the host. Specification includes effects of ground offset voltage.

2.6 Electrical Power Supply Characteristics

Parameter	Symbol	Min	Typ.	Max	Units
Power Supply Voltage	V_{CC1} , V_{CCTx}, V_{CCRx}	3.13	3.30	3.47	V
Power Consumption	P_W	-	-	10	W
Power Consumption-LP mode	-	-	-	1.5	W

Notes:
The specified characteristics are met within the recommended range of operation. Unless otherwise noted typical data are quoted at nominal voltage and +25°C ambient temperature.

2.7 Laser Safety:

All transceivers are Class 1 Laser products per FDA/CDRH and IEC-60825 standards. They must be operated under specified operating conditions.

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3 Pinout Information

3.1 Electrical Pin Definition

Host	Module	Logic	Symbol	Description	Plug	Notes
1	1		GND	Ground	1	1
2			GND	Ground	1	1
3	2	CML-I	Tx2n	Transmitter	3	
4	3	CML-I	Tx2p	Transmitter Non-	3	
5	4		GND	Ground	1	1
6			GND	Ground	1	1
7	5	CML-I	Tx4n	Transmitter	3	
8	6	CML-I	Tx4p	Transmitter Non-	3	
9	7		GND	Ground	1	1
10			GND	Ground	1	1
11	8	LVTTL-I	ModSelL	Select	3	
12	9	LVTTL-I	ResetL	Reset	3	
13	10		Vcc Rx	+3.3 V Power	2	2
14			Vcc Rx	+3.3 V Power	2	2
15	11	LVCMOSI/O	SCL	2-wire serial	3	
16	12	LVCMOSI/O	SDA	2-wire serial	3	
17	13		GND	Ground	1	1
18			GND	Ground	1	1
19	14	CML-O	Rx3p	Receiver Non-	3	
20	15	CML-O	Rx3n	Receiver Inverted	3	
21	16		GND	Ground	1	1
22			GND	Ground	1	1
23	17	CML-O	Rx1p	Receiver Non-	3	
24	18	CML-O	Rx1n	Receiver Inverted	3	
25	19		GND	Ground	1	1
26			GND	Ground	1	1
27	20		GND	Ground	1	1
28			GND	Ground	1	1
29	21	CML-O	Rx2n	Receiver Inverted	3	
30	22	CML-O	Rx2p	Receiver Non-	3	
31	23		GND	Ground	1	1
32			GND	Ground	1	1
33	24	CML-O	Rx4n	Receiver Inverted	3	
34	25	CML-O	Rx4p	Receiver Non-	3	
35	26		GND	Ground	1	1
36			GND	Ground	1	1
37	27	LVTTL-O	ModPrsL	Presen	3	
38	28	LVTTL-O	IntL/RxLOS	Interrupt/optional	3	

Host	Module	Logic	Symbol	Description	Plug	Notes
39	29		Vcc Tx	+3.3 V Power	2	2
40			Vcc Tx	+3.3 V Power	2	2
41	30		Vcc1	+3.3 V Power	2	2
42	31	LVTTL-I	LPMode/Tx	Low Power	3	
43	32		GND	Ground	1	1
44			GND	Ground	1	1
45	33	CML-I	Tx3p	Transmitter Non-	3	
46	34	CML-I	Tx3n	Transmitter	3	
47	35		GND	Ground	1	1
48			GND	Ground	1	1
49	36	CML-I	Tx1p	Transmitter Non-	3	
50	37	CML-I	Tx1n	Transmitter	3	
51	38		GND	Ground	1	1
52			GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements, defined for the host side of the Host Edge Card Connector, are listed in Table 4. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx, Vcc1and Vcc Tx may be internally connected within the QSFP112 module in any combination. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

3.2 Connector Pad Layout

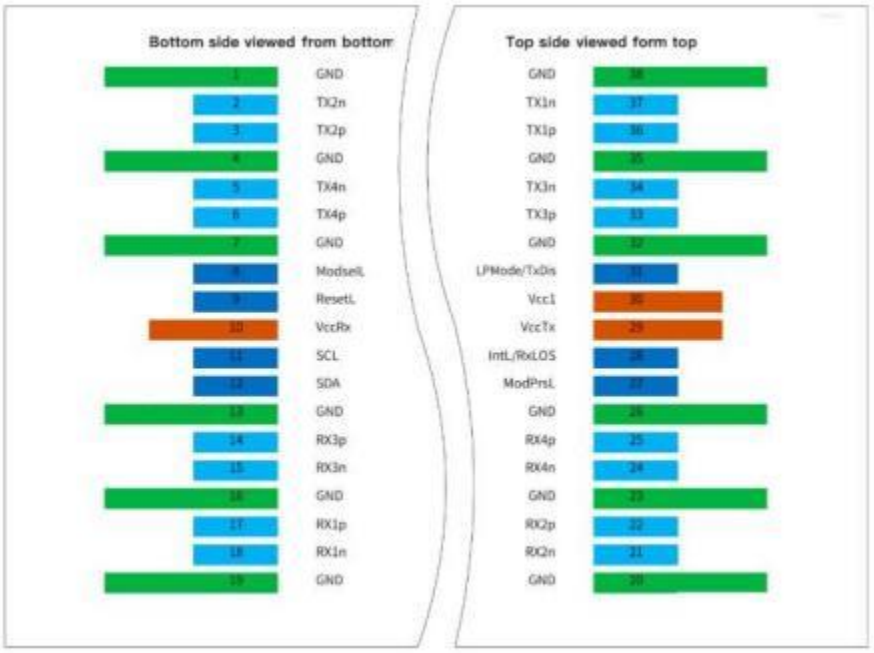

Figure 1 QSFP112 Module contact assignment

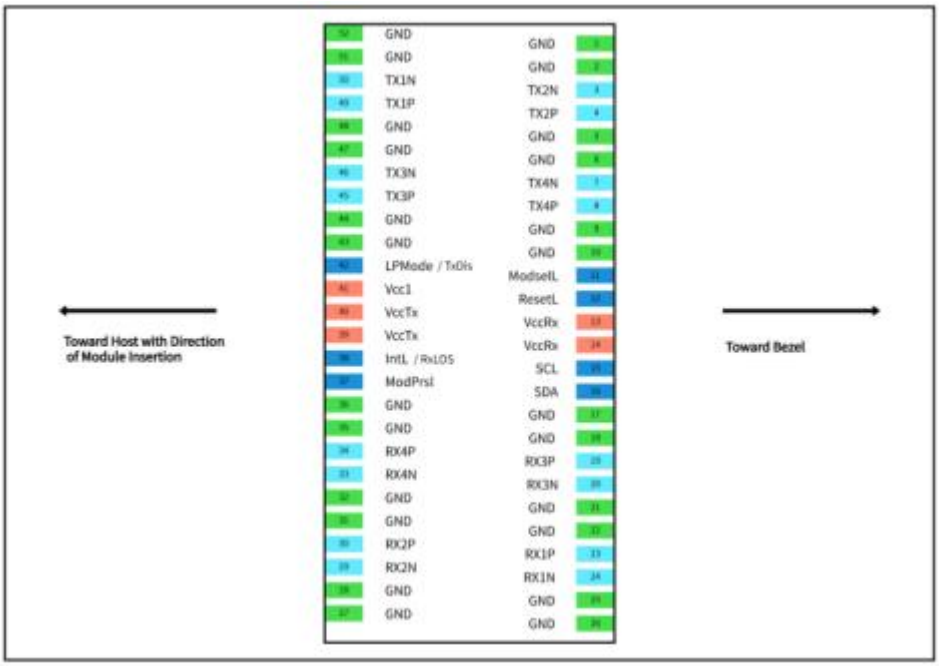

Figure 2 QSFP112 Host PCB pad assignment

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3.3 Application Notes

Low Speed Electrical Hardware Pins: In addition to the two wire interface (TWI) serial interface the module has the following low speed pins for control and status: a) ModSelL b) LPMode/TxDis c) ResetL d) ModPrsL e) IntL/RxLOS .

ModSelL: The ModSelL is an input pin. When held low by the host, the module responds to TWI serial communication commands. The ModSelL allows the use of multiple QSFP112 modules on a single TWI bus. When the ModSelL is "High", the module shall not respond to or acknowledge any TWI communication from the host. ModSelL signal input node must be biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt TWI communications within the ModSelL de-assert time after any QSFP112 modules are deselected. Similarly, the host must wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL: The ResetL pin must be pulled to Vcc in the QSFP112 module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

LPMode/TxDis: LPMode/TxDis is a dual-mode input signal from the host operating with active high logic. It shall be pulled towards Vcc in the module. At power-up or after ResetL is deasserted LPMode/TxDis behaves as LPMode. If supported, LPMode/TxDis can be configured as TxDis using the TWI except during the execution of a reset. Timing requirements for LPMode/TxDis mode changes are found in, see Table 15. LPMode is used in the control of the module power mode, see CMIS Chapter 6.3.1.3. When LPMode/TxDis is configured as LPMode, the module behaves as though TxDis=0. By using the LPMode signal and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits the host controls how much power a module can consume. When LPMode/TxDis is configured as TxDis, the module behaves as though LPMode=0. In this mode LPMode/TxDis when set to 1 or 0 disables or enables all optical transmitters within the times specified in Table 15. Changing LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is high disables all optical transmitters. If the module was in low power mode, then the

module transitions out of low power mode at the same time. If the module is already in high power state (Power Override control bits) with transmitters already enabled, the module shall disable all optical transmitters. Changing the LPMode/TxDis mode from LPMode to TxDis when the LPMode/TxDis state is low, simply changes the behavior of the mode of LPMode/TxDis. The behavior of the module depends on the Power Override control bits. Note that the "soft" functions of TxDis, LPMode, IntL and RxLOSL allow the host to poll or set these values over the TWI as an alternative to monitoring/setting signal values. Asserting either the "hardware" or "soft bit" (or both) for TxDis or LPMode results in that function being asserted.

ModPrsL: ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted"Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

IntL/RxLOSL: IntL/RxLOSL is a dual-mode active-low, open-collector output signal from the module. It shall be pulled up towards Vcc on the host board (see Table 4). At power-up or after ResetL is released to high, IntL/RxLOSL is configured as IntL. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the TWI serial interface. The IntL signal is deasserted "High" after all set interrupt flags are read. If dual mode operation supported, IntL/RxLOSL can be optionally programmed as RxLOSL using the TWI except during the execution of a reset. If the module has no interrupt flags asserted (IntL/RxLOSL is high), there should be no change in IntL/RxLOSL states after the mode change. If IntL/RxLOSL is configured as RxLOSL, a low indicates that there is a loss of received optical power on at least one lane. "high" indicates that there is no loss of received optical power. Timing requirements for IntL/RxLOSL including fast RxLOS mode are found in Table 15. The actual condition of loss of optical receive power is specified by other governing documents, as the alarm threshold level is application specific. The module shall pull RxLOSL to low if any lane in a multiple lane module or cable has a LOS condition and shall release RxLOSL to high only if no lane has a LOS condition. Editor's Note: registers to support optional RxLOSL will be added in future revisions of CMIS.

Low Speed Electrical Specification: Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc. Vcc refers to the generic supply voltages of VccTx, VccRx, Vcc_host or Vcc1. Hosts shall use a pull-up resistor connected to Vcc_host on each of the TWI SCL (clock), SDA (data), and all low speed status outputs. The SCL and SDA is a hot plug interface that may support a bus topology. During module insertion or removal, the module may implement a pre-charge circuit which prevents corrupting data transfers from other modules that are already using the bus. The QSFP112 low speed electrical

specifications are given in Table 4. This specification ensures compatibility between host bus masters and the TWI.

High Speed Electrical Specification:

Rx(n)(p/n): Rx(n)(p/n) are QSFP112 module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC(SerDes). The AC coupling is inside the QSFP112 module and not required on the Host board. When properly terminated, the differential voltage swing shall be less than or equal to 900 mVpp or the relevant standard, whichever is less. Output squelch for loss of optical input signal, hereafter Rx Squelch, is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, then the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output. In the squelched state output impedance levels are maintained while the differential voltage amplitude shall be less than 50 mVpp. In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the TWI serial interface. Rx Squelch Disable is an optional function.

Tx(n)(p/n): Tx(n)(p/n) are QSFP112 module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP112 optical module. The AC coupling is implemented inside the QSFP112 optical module and not required on the Host board. Output squelch for loss of electrical signal, hereafter Tx Squelch, is an optional function. Where implemented it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 70 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel, the loss of any of the incoming electrical input channels causes the optical output channel to be squelched. For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended. In module operation, where Tx Squelch is implemented, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the TWI serial interface. Tx Squelch and Tx Squelch Disable are optional functions.

4 Digital Diagnostic Specification

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transceiver Case Temperature	DMI_Temp	-3		+3	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	-3%		+3%	V	Full operating range
Channel RX power monitor absolute error	DMI_RX	-3		+3	dB	Per channel
Channel Bias current monitor	DMI_Ibias	-10%		+10%	mA	Per channel
Channel TX power monitor absolute error	DMI_TX	-3		+3	dB	Per channel

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5 Memory Map-4.0

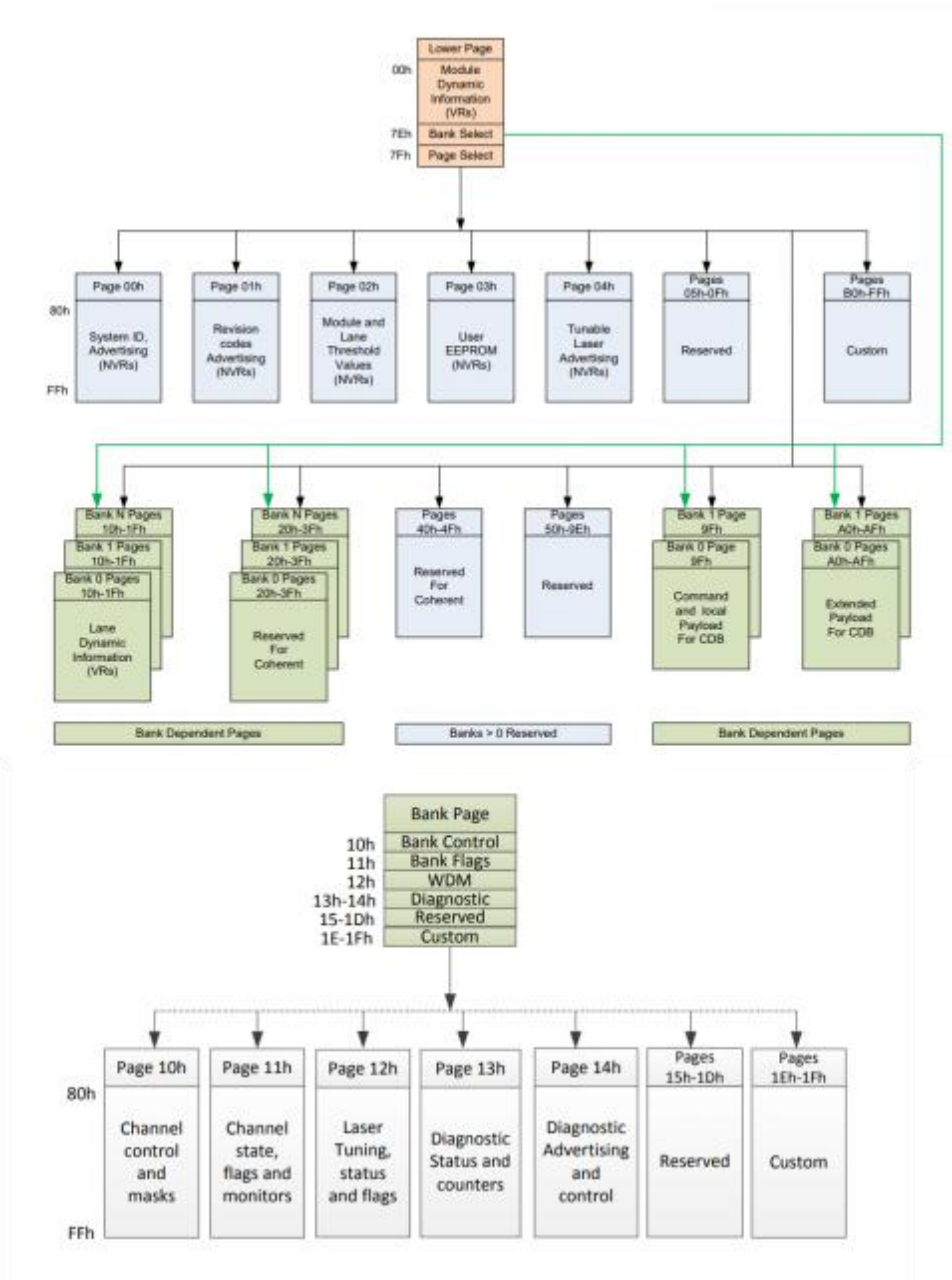

Figure 3 - QSFP112 Memory Map

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6 OPTICAL INTERFACE LANES AND ASSIGNMENT

The recommended location and numbering of the optical ports for 3 Media Dependent Interfaces (MDI) are shown in Figure 4. The transmit and receive optical lanes shall occupy the positions depicted in Figure 4 when looking into the MDI receptacle with the connector keyway feature on top.

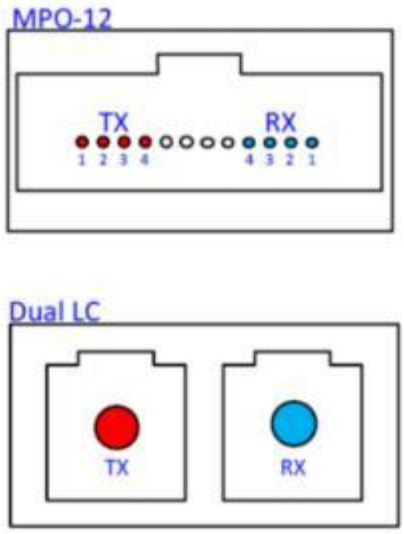

Figure 4 -Optical media dependent interface port assignment

7 Mechanical Specifications

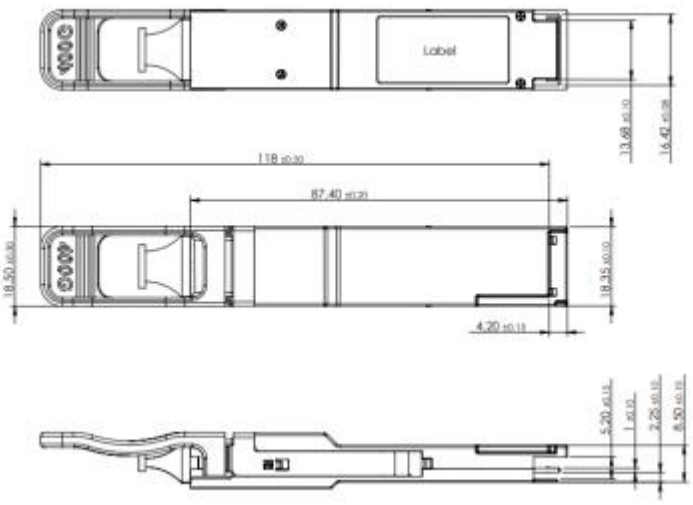

Figure 5 - QSFP112 Mechanical Specifications

Notes:
All dimensions shown are in millimetres.
Tolerances are in accordance with QSFP112 MSA.

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8 Ordering Information

Ccloud PN	Operating Temperature	Wavelength	Reach	Latch Color
CC-QCS110M-SD	0。C to 70。C	850nm	100m	Beige

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