

400G QSFP112 DR4 Optical Transceiver

CC-QSFP04DR4-12D

Features

- Silicon photonics integrated solution
- Hot-pluggable QSFP112
- MPO-12 APC
- Up to 500 meters reach on single-mode fiber
- 4x106.25 Gb/s electrical interface



Applications

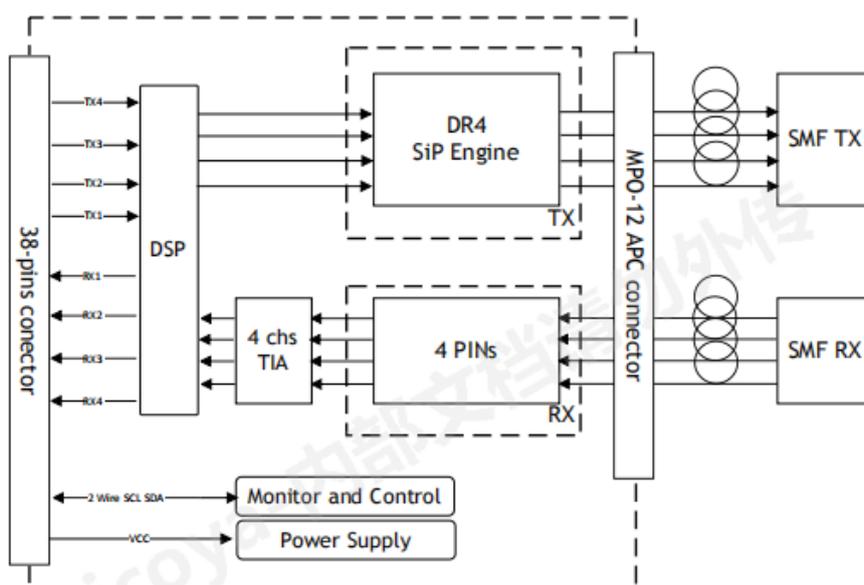
- Data centers and cloud networks
- 400G Ethernet

DESCRIPTION

CC-QSFP04DR4-12D optical transceiver is a full duplex, silicon-photonics-based optical transceiver that provides a high-speed link at an aggregated data rate of Gigabit per second (Gb/s) over 500 meters on single-mode fibers (SMF). This product offers a high-density 400 Gb/s Ethernet connectivity solution for data centers, high-performance computing networks, enterprise core and distribution layers, and service provider transport applications. Our transceiver modules are designed to meet commercial temperature application environments and to be compliant with all applicable standards.

FUNCTIONAL DESCRIPTION

The CC-QSFP04DR4-12D contains an MPO-12 APC connector for the optical interface and a 38-pins connector for the electrical interface. The chart in Figure shows the functional block diagram of this product.



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Transmitter Operation

The transceiver module receives 4 channels of 106.25 Gb/s electrical data, which are processed by optical DSP with CDR functions, that reshape and reduce the jitter of each electrical signal.

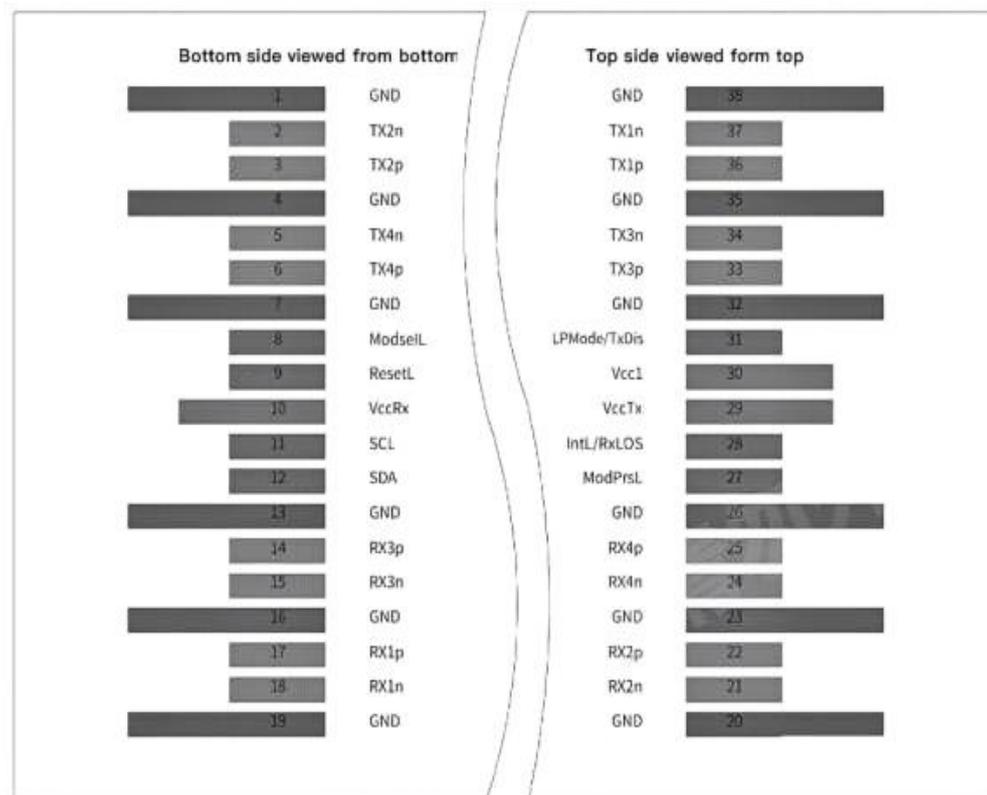
Subsequently, the integrated Ccloud silicon photonics engine converts each channel to one of the 4 optical signals. And total outputs deliver a total data rate of 400 Gb/s over 4 parallel single mode fibers .

Receiver Operation

The receiver section take the optical input of 400Gb/s signals over 4 parallel single mode fibers. Each optical signal is converted to an electrical signal by one of the 4 PIN photodiodes (PINs) followed by trans-impedance amplifiers (TIAs). All 4 electrical signals are fed to the optical DSP with CDR functions to reshape and retime each electrical signal as one of the 4 output channels.

IDENTIFICATION OF PINOUT ASSIGNMENT

The transceiver board has 38 pins arranged in the top and bottom rows. The pin map is shown in Table below. The pin orientation is shown below in Figure.



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Pin

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter inverted Data input	3	
3	CML-I	Tx2p	Transmitter Non-inverted Data input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Select	3	
9	LVTTL-I	ResetL	Reset	3	
10		Vcc Rx	+3.3 V Power supply receiver	2	2
11	LVC MOS-I/O	SCL	2-wire serial interface clock	3	
12	LVC MOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Present	3	
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	3	
29		Vcc Tx	+3.3 V Power supply transmitter	2	2
30		Vcc1	+3.3 V Power Supply	2	2
31	LVTTL-I	LPMoDe/Tx Dis	Low Power Mode/optional TX	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	

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35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP112 module. All are common within the QSFP112 module and all voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. The connector pins are each rated for a maximum current of 1.5A (max. current of 2.0 A is required for high module power of 15-20W).

ABSOLUTE MAXIMUM RATINGS

Environmental

Parameter	Symbol	Min	Max	Unit	Note
Storage and Transportation Temperature	Ts	-40	+85	°C	
Relative Humidity	RH	5	+85	%	1
Operating Case Temperature	Top	0	+70	°C	

Note:

1. Non-condensing.

Electrical

Parameter	Symbol	Min	Max	Unit	Note
+3.3V Power Supply Voltage		-0.3	+3.465	V	

Optical

Parameter	Symbol	Min	Max	Unit	Note
RX damage threshold, per Lane	P _{Rdmg}	+5		dBm	

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit	Note
Relative Humidity	RH	5	+85	%	1
Operating Case Temperature	Top	0	+70	°C	
Operation Supply Voltage	V	3.135	3.465	V	
Data Rate, Each Lane			53.125	Gbd	PAM4
Data Rate Accuracy		-100	+100	ppm	
Pre-FEC Bit Error Ratio			2.4E-4		
Link Distance with SMF			500	m	2

Note:

1. Non-condensing.
2. FEC required on the host system to support maximum distance.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated the following parameters and performances are over the full range of operating conditions defined in section 5, over the entire wavelength range. The typical values are referenced to case temperature of +35 oC, nominal power supply, and end of life.

Parameter	Symbol	Min.	Typ.	Max.	Units	Ref.
Transmitter						
Signaling Rate per Lane			53.125 ± 100 ppm		GBd	
Receiver						
Signaling Rate per Lane			53.125 ± 100 ppm		GBd	
Operation						
Supply Voltage	Vcc	3.135		3.465	V	
Supply Current	Icc			2.9	A	
Module total power	P			9	W	

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Transmitter						
Signaling Rate per Lane		53.125 ± 100 ppm			GBd	
Lane Center Wavelengths (range)	L	1304.5		1317.5	nm	
Modulation Format		PAM4				
Side-mode Suppression ratio (SMSR)	SMSR	30			dB	
Average Launch Power, each Lane		-2.9		4	dBm	
Outer Optical Modulation Amplitude, (OMA outer), each Lane	OMA	-0.8		4.2	dBm	
Launch power in OMA outer minus TDECQ, each Lane		-2.2			dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane				3.4	dB	
Optical Extinction Ratio, each Lane	ER	3.5			dB	
Optical Return Loss Tolerance, each Lane				21.4	dB	
Receiver						
Signaling Rate per Lane		53.125 ± 100 ppm			GBd	
Lane Center Wavelengths (Range)	L	1304.5		1317.5	nm	
Modulation Format		PAM4				
Average Receive Power, each Lane		-5.9		4	dBm	
Receive Power (OMA outer), each Lane				4.2	dBm	
Receiver Reflectance, each Lane				-26	dB	
Stressed Receiver Sensitivity (OMA outer), each Lane				-1.9	dBm	
Receiver Sensitivity (OMA outer), each Lane				-3.9	dBm	

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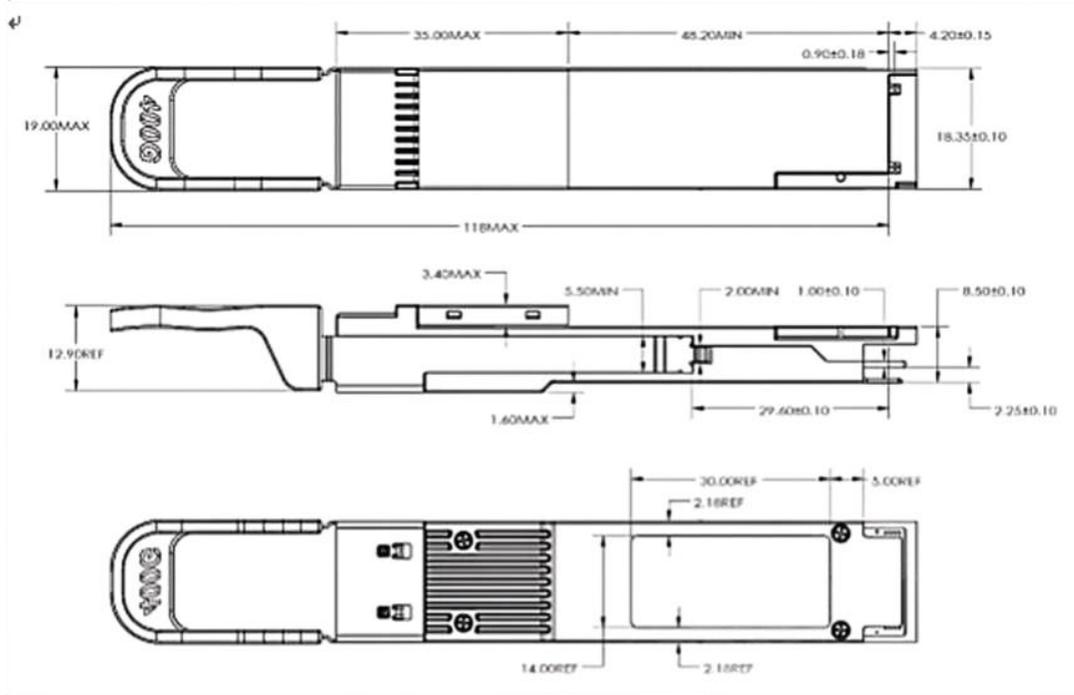
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Module outline drawing



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