800G OSFP DR8 Transceiver
CC-OSFP08DR8-12D

Features

- OSFP Package
- 3.3V power supply
- Dual MTP8 APC optical receptacle connector
- Hot pluggable
- 2x30 OSFP Electrical Interface
- Refer to *OSFP Octal Small From Factor Pluggable Module R5.05*
- Comply with *Common Management Interface Specification for 8-16x Plug- gable Transceivers, R5.2*
- SMF Fiber

Applications

- High performance computing interconnect
- Data Centers
- 800G DR8, 2x400G DR4, 8x100G DR1

Optical Transmitter

- 1304.5~1317.5nm EML
- 53GBaud data rate
- LVCML AC Coupled input

Optical Receiver

- 1304.5~1317.5nm PIN PD Receiver
- 53GBaud data rate
- LVCML AC Coupled output

Control and Monitor Interface

- Low Power Mode
- Module Present
- Module Interrupt
- Module Reset

Case Operating Temperature:

- Commercial: 0 to 70°C

I^2C Serial Data

- SCL Serial Clock Input
- SDA Serial Data I/O

Description

The CC-OSFP08DR8-12D is an 8x100Gbps optical transceivers in an OSFP housing. It is designed to support the next generation 800Gbps applica- tion used inside the Datacenter. The module is configured with 8 lanes optics which is using the 53GBaud 1310nm EML transmitters the 53GBaud high sensitivity PIN PD receivers. It is compliant with the of OSFP MSA specifications. It operates at 53.125GBaud up to 500m over single-mode fiber.

The module comply with Common Management Interface Specification for 8/16x Pluggable Transceivers,R5.2.

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Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	T_S	-40	+85	ºC	Exceeding the Absolute Maximum Ratings may cause irreversible damage to the device.The device is not intended to be operated under the condition of simultaneous Absolute Maximum Ratings, a condition which may cause irreversible damage to the device.RH is Non-condensing condition.
Relative Humidity - Storage	RH_S	0	95	%	
Relative Humidity - Operating	RH_O	0	85	%	
Supply Voltage	V_{CC}	-0.5	3.6	V	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Operating Case Temperature	T_{OPR}	0	25	70	ºC	Temperature Range = C
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Power Consumption	Pcon	-		14.6	W	
PAM4 Signaling rate, each lane	S	-	53.125	-	GBaud	range：±100ppm

Transmitter Electrical Interfaces

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Tx_Data Differential Input Voltage	V_{IN}	-	-	880	mV	
Tx_Data Differential Input Impedance	Z_{IN}	-	100	-	Ω	
Signaling rate per lane	S	-	53.125	-	GBaud	range：±100ppm

Receiver Electrical Interfaces

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Rx_Data Differential Output Voltage	V_{OUT}	-	-	900	mV	
Rx_Data Differential Output Impedance	Z_{OUT}	-	100	-	Ω	
Signaling rate per lane	S	-	53.125	-	GBaud	range：±100ppm

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Transmitter Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Signaling rate each lane		53.125±100ppm			GBd	
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Laser Type		EML				
Side-mode Suppression Ration	SMSR	30				
Average Launch Power, each lane	AOP_L	-2.9	-	4.0	dBm	
Outer Optical Modulation Amplitude	OMA_{outer}	0.2	-	4.2	dBm	For TDECQ＜1.4dB
		-1.2+TDECQ		4.2	dBm	For 1.4dB≤TDECQ≤3.4dB
Transmitter and Dispersion Penalty Eye Closure for PAM4	TDECQ	-	-	3.4	dB	Note 1
Optical Output with Tx OFF, each lane	P_{OFF}	-	-	-15	dBm	
Extinction Ratio	ER	3.5	-	-	dB	Note 1
Transmit Reflectance	RFL	-	-	-26	dB	
Note 1: Test with SSPRQ pattern.						

Receiver Optical Specifications

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Signaling rate each lane		53.125±100ppm			GBd	
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Receiver Sensitivity (OMA_{outer}), each lane	SEN	-	-	-2.9	dBm	Each Lane (Note1)
Average receive power	P_{IN}	-5.9	-	4	dBm	Each Lane
Damage threshold		5	-	-	dBm	Each Lane
Receive Reflectance	RFL	-	-	-26	dB	
Note 1: BER = 1E-8@-2.9dBm(Non-stressed RX Sensitivity OMAouter) BER = 2.4E-4 , PAM4 Signaling rate （each lane) 53.125GBaud, and PRBS 2^{31}-1						

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
High power mode to Low power mode tran- sition time from assertion of M_LPWn or M_RSTn or ForceLowPwr	T_hplp		-	500	us	
Min Reset Assert Duration	t_reset_init	500	-		us	

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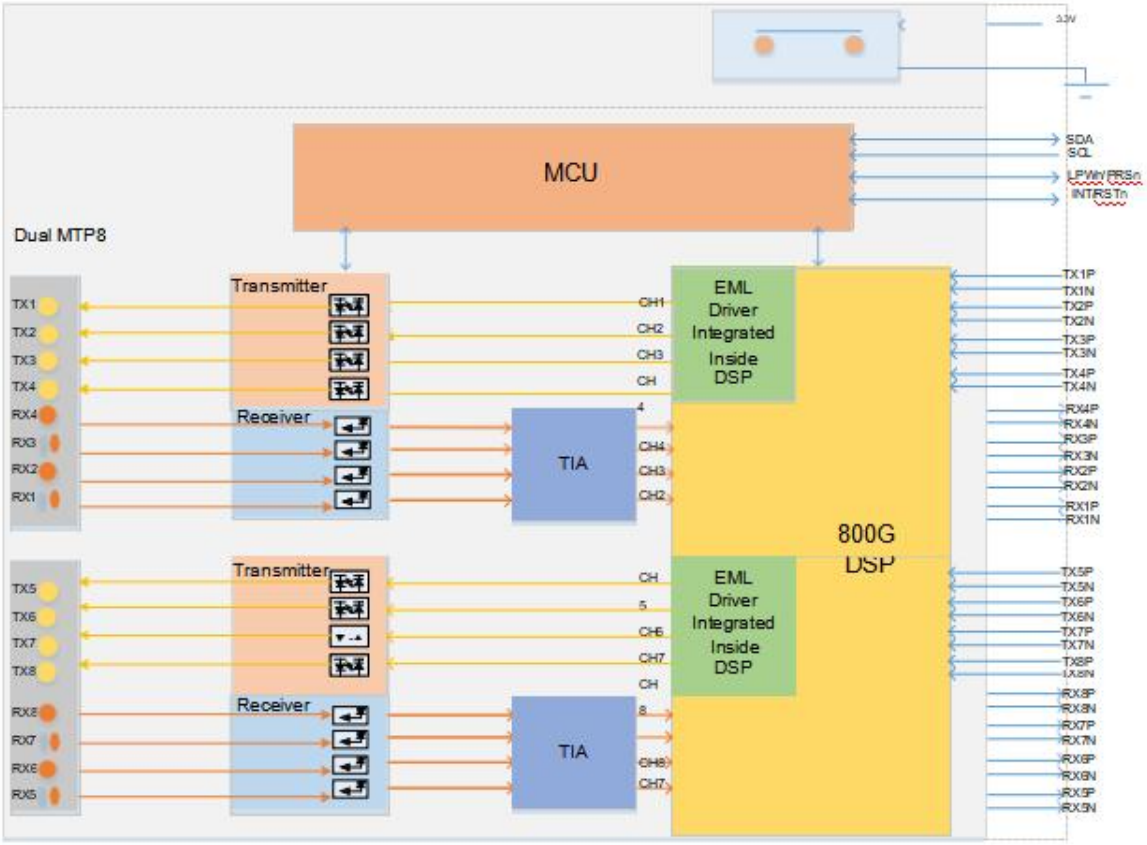
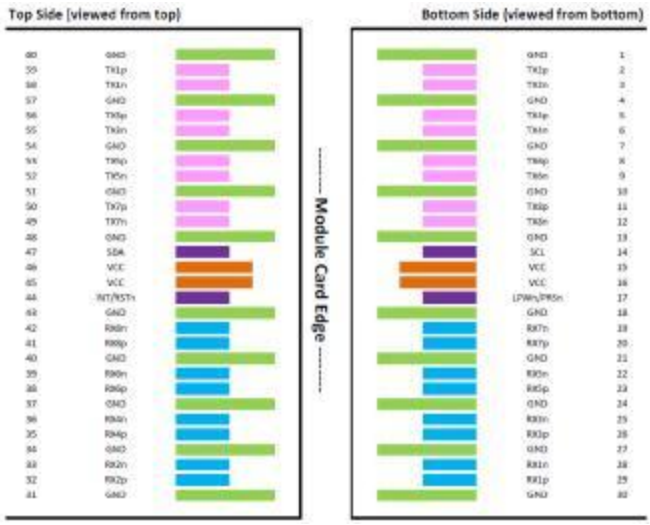
Module Block Diagram



Pin Definitions



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Pin Description

Pin#	Logic	Symbol	Description	Direction	Plug Sequence	Notes
1		GND	Module Ground		1	
2	CML-I	TX2P	CH2 Transmitter Date Non-Inverted	Input from Host	3	
3	CML-I	TX2N	CH2 Transmitter Date Inverted	Input from Host	3	
4		GND	Module Ground		1	
5	CML-I	TX4P	CH4 Transmitter Date Non-Inverted	Input from Host	3	
6	CML-I	TX4N	CH4 Transmitter Date Inverted	Input from Host	3	
7		GND	Module Ground		1	
8	CML-I	TX6P	CH6 Transmitter Date Non-Inverted	Input from Host	3	
9	CML-I	TX6N	CH6 Transmitter Date Inverted	Input from Host	3	
10		GND	Module Ground		2	
11	CML-I	TX8P	CH8 Transmitter Date Non-Inverted	Input from Host	3	
12	CML-I	TX8N	CH8 Transmitter Date Inverted	Input from Host	3	
13		GND	Module Ground		1	
14	LVCMOS-I/O	SCL	2-wire Serial Interface clock	Bi-Directional	3	A
15		VCC	+3.3V Power Supply	Power from Host	3	
16		VCC	+3.3V Power Supply	Power from Host	1	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present	Bi-Directional	3	B
18		GND	Module Ground		3	
19	CML-O	RX7N	CH7 Receiver Date Inverted	Output to Host	1	
20	CML-O	RX7P	CH7 Receiver Date No-Inverted	Output to Host	1	
21		GND	Module Ground		3	
22	CML-O	RX5N	CH5 Receiver Date Inverted	Output to Host	3	
23	CML-O	RX5P	CH5 Receiver Date No-Inverted	Output to Host	1	
24	CML-O	GND	Module Ground		3	
25	CML-O	RX3N	CH3 Receiver Date Inverted	Output to Host	3	
26		RX3P	CH3 Receiver Date No-Inverted	Output to Host	3	
27	CML-O	GND	Module Ground		1	
28	CML-O	RX1N	CH1 Receiver Date Inverted	Output to Host	3	
29		RX1P	CH1 Receiver Date No-Inverted	Output to Host	3	
30		GND	Module Ground		1	
31	CML-O	GND	Module Ground		1	
32	CML-O	RX2P	CH2 Receiver Date Non-Inverted	Output to Host	3	
33		RX2N	CH2 Receiver Date Inverted	Output to Host	3	
34	CML-O	GND	Module Ground		1	
35	CML-O	RX4P	CH4 Receiver Date Non-Inverted	Output to Host	3	

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Pin#	Logic	Symbol	Description	Direction	Plug Sequence	Notes
36	CML-O	RX4N	CH4 Receiver Date Inverted	Output to Host	3	
37		GND	Module Ground		1	
38	CML-O	RX6P	CH6 Receiver Date Non-Inverted	Output to Host	3	
39	CML-O	RX6N	CH6 Receiver Date Inverted	Output to Host	3	
40		GND	Module Ground		1	
41	CML-O	RX8P	CH8 Receiver Date Non-Inverted	Output to Host	3	
42	CML-O	RX8N	CH8 Receiver Date Inverted	Output to Host	3	
43		GND	Module Ground		1	
44	Multi-Level	INT/RSTn	Module Interrupt/Module Reset	Bi-Directional	3	C
45		VCC	+3.3V Power Supply	Power from Host	2	
46		VCC	+3.3V Power Supply	Power from Host	2	
47	LVCMOS-I/O	SDA	2-wire Serial Interface data	Bi-Directional	3	A
48		GND	Module Ground		1	
49	CML-I	TX7N	CH7 Transmitter Date Inverted	Input from Host	3	
50	CML-I	TX7P	CH7 Transmitter Date Non-Inverted	Input from Host	3	
51		GND	Module Ground		1	
52	CML-I	TX5N	CH5 Transmitter Date Inverted	Input from Host	3	
53	CML-I	TX5P	CH5 Transmitter Date Non-Inverted	Input from Host	3	
54		GND	Module Ground		1	
55	CML-I	TX3N	CH3 Transmitter Date Inverted	Input from Host	3	
56	CML-I	TX3P	CH3 Transmitter Date Non-Inverted	Input from Host	3	
57		GND	Module Ground		1	
58	CML-I	TX1N	CH1 Transmitter Date Inverted	Input from Host	3	
59	CML-I	TX1P	CH1 Transmitter Date Non-Inverted	Input from Host	3	
60		GND	Module Ground		1	
Note A	Open-Drain with Pull-up resistor on Host					
Note B	LPWn/PRSn is a dual function signal that allows the host to signal Low Power mode and the module to indicate Module Present.					
Note C	INT/RSTn is a dual function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module.					

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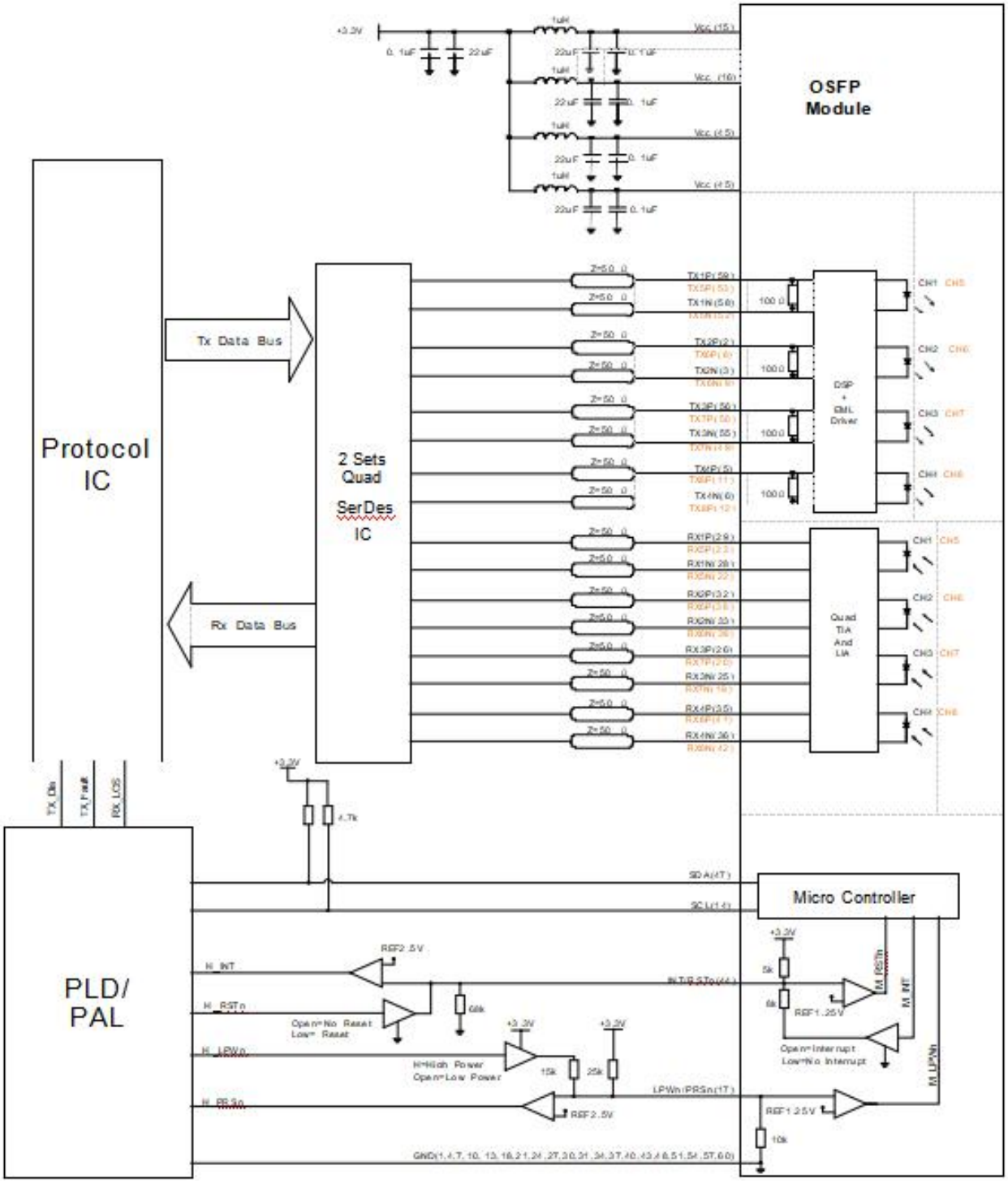
Host Board and Module Board Diagram



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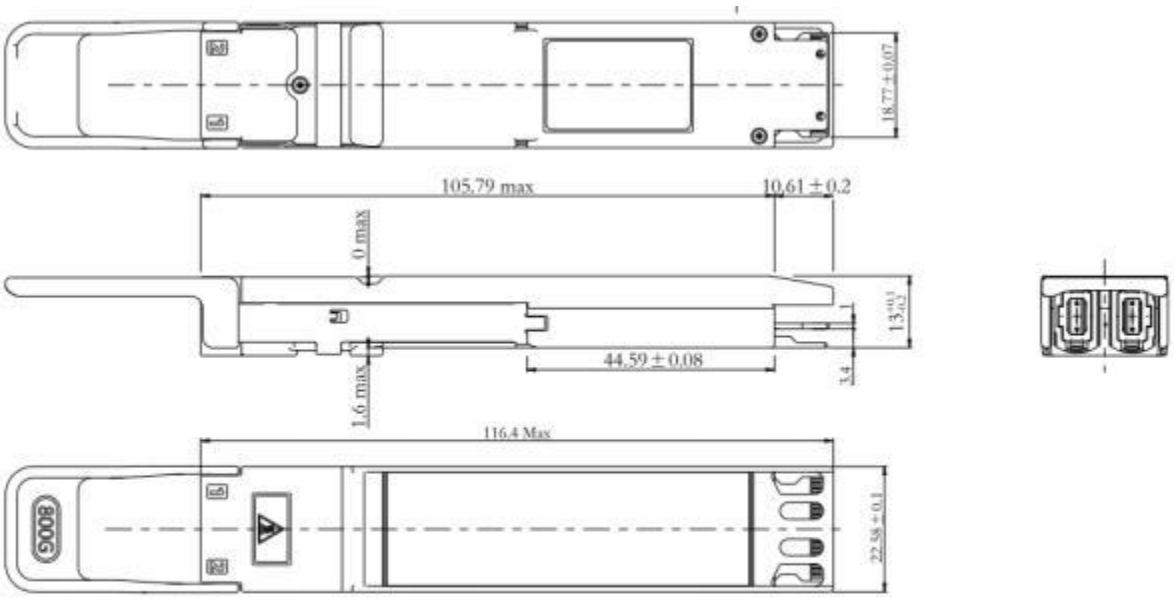
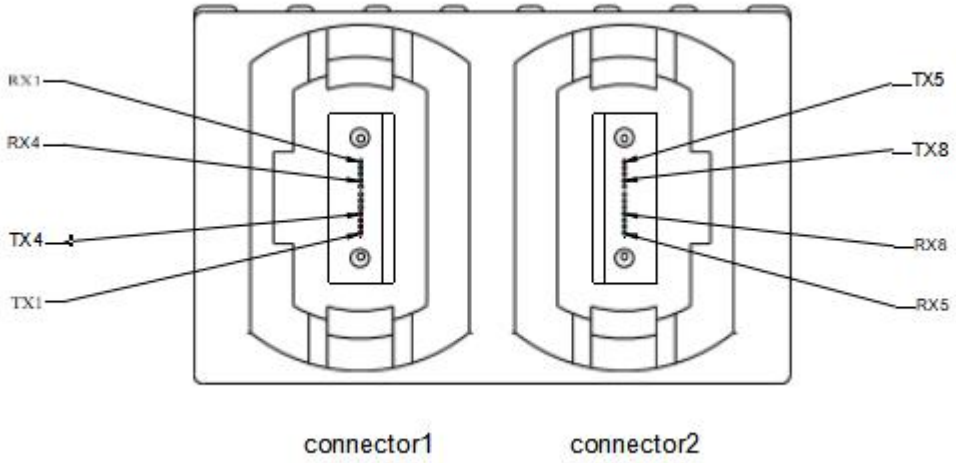
Mechanical Specifications



NOTES:
1.TOLERANCE: ±0.1mm.
2.OTHERS ACCORDING WITH OSFP MSA OR CUSTOMER SPEC.
3.OPTICAL PORT ACCORDING WITH Dual MPO CONNECTOR SPEC.

Optical Lane Assignment



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Appendix A Document Revision

Version No.	Date	Description
V Draft	2024-06-10	Draft release

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